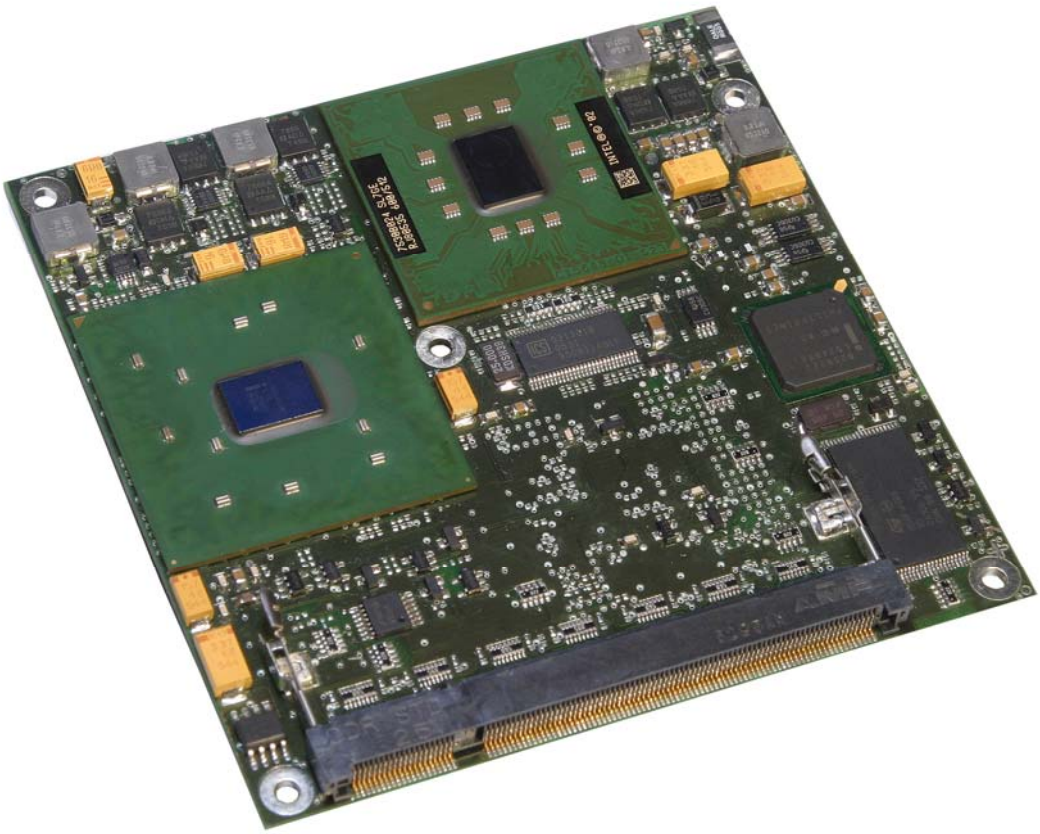
Kontron User's Guide



microETXexpress™-PM

Document Revision 1.11

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1 User Information

1.1 About This Manual

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- IBM, XT, AT, PS/2 and Personal System/2 are trademarks of International Business Machines Corp.
- Microsoft is a registered trademark of Microsoft Corp.
- Intel is a registered trademark of Intel Corp.
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1.4 Standards

Kontron Embedded Modules GmbH is certified to ISO 9000 standards.

1.5 Warranty

This Kontron Embedded Modules GmbH product is warranted against defects in material and workmanship for the warranty period from the date of shipment. During the warranty period, Kontron Embedded Modules GmbH will at its discretion decide to repair or replace defective products.

Within the warranty period, the repair of products is free of charge as long as warranty conditions are observed.

The warranty does not apply to defects resulting from improper or inadequate maintenance or handling by the buyer, unauthorized modification or misuse, operation outside of the product's environmental specifications or improper installation or maintenance.

Kontron Embedded Modules GmbH will not be responsible for any defects or damages to other products not supplied by Kontron Embedded Modules GmbH that are caused by a faulty Kontron Embedded Modules GmbH product.

1.6 Technical Support

Technicians and engineers from Kontron Embedded Modules GmbH and/or its subsidiaries are available for technical support. We are committed to making our product easy to use and will help you use our products in your systems.

Before contacting Kontron Embedded Modules GmbH technical support, please consult our Web site at http://www.kontron-emea.com/emd for the latest product documentation, utilities, and drivers. If the information does not help solve the problem, contact us by telephone or email.

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2 Introduction

2.1 microETXexpress™-PM

The microETXexpress™-PM component SBC modules hosts Intel® Pentium® M Processor in combination with an Intel® 855GM/GME or Intel® 852GM chipset with an integrated graphics memory controller hub with Intel® Extreme Graphics 2 technology. Celeron M versions of this board are possible, too. A DDR-SODIMM socket can hold either PC1600 ,PC2100 or PC2700 DDR memory modules up to 1GB. Furthermore six USB 2.0 ports and one 10/100 MBit Ethernet interface completes the interfaces.

2.2 ETXexpress® Documentation

This product manual serves as one of three principal references for an ETXexpress® design. It documents the specifications and features of micro*ETXexpress™-PM*. The other two references, which are available from the Kontron Embedded Modules Web site, include:

- The *ETXexpress® Component SBC™ and COMexpress Specification* defines the ETXexpress® module form factor, pinout, and signals.
- The *ETXexpress® Component SBC™ Design Guide* serves as a general guide for baseboard design, with a focus on maximum flexibility to accommodate a range of ETXexpress® modules.

Note: Some of the information contained within this product manual applies only to certain product revisions (Prev: xxx). If certain information applies to specific product revisions (Prev: xxx) it will be stated. Please check the product revision of your module to see if this information is applicable.

2.3 ETXexpress® Benefits

Micro Embedded technology extended express (microETXexpress™) modules are very compact (95 x 95 mm, 12mm thick), highly integrated computers. All microETXexpress™ modules feature a standardized form factor and a standardized connector layout that carry a specified set of signals. Each ETXexpress® module is based on connector type 2 of the COMexpress specification. This standardization allows designers to create a single-system baseboard that can accept present and future ETXexpress® modules.

ETXexpress® modules include common personal computer (PC) peripheral functions such as:

- Graphics
- Parallel, Serial, and USB ports
- Keyboard/mouse
- Ethernet
- Sound
- IDE (and SATA)

The baseboard designer can optimize exactly how each of these functions implements physically. Designers can place connectors precisely where needed for the application on a baseboard designed to optimally fit a system's packaging.

A peripheral PCI bus can be implemented directly on the baseboard rather than on mechanically unwieldy expansion cards. The ability to build a system on a single baseboard using the computer as one plug-in component simplifies packaging, eliminates cabling, and significantly reduces system-level cost.

A single baseboard design can use a range of ETXexpress® modules. This flexibility can differentiate products at various price/performance points, or to design future proof systems that have a built-in upgrade path. The modularity of an ETXexpress® solution also ensures against obsolescence as computer technology evolves. A properly designed ETXexpress® baseboard can work with several successive generations of ETXexpress® modules.

An ETXexpress® baseboard design has many advantages of a custom, computer-board design but delivers better obsolescence protection, greatly reduced engineering effort, and faster time to market.

3 Specifications

3.1 Functional Specifications

Processor: Mobile Intel® Pentium® M

- Intel® Pentium® M Processor 738 1,4 GHz (see section Important Information)
- Intel Celeron® M Processor 373 0.6 GHz - 1.0 GHz (see section Important Information)
- Cache: On-die Second level 2 MB(1.4 GHz) 512 kB (Celeron M 0.8 GHz, 1.0 GHz), 0 kB (600 MHz and 800 MHz cacheless)
- Supports Intel® Architecture with Dynamic Execution
- High performance, low-power core
- On-die, primary 32-kbyte instruction cache and 32-kbyte write-back data cache
- On-die, up to 2-Mbyte second level cache with Advanced Transfer Cache Architecture
- Advanced Branch Prediction and Data Prefetch Logic
- Streaming SIMD Extensions 2 (SSE2)
- 400-MHz, Source-Synchronous processor system bus
- Advanced Power Management features including Enhanced Intel SpeedStep® technology

Chipset: Intel® 852GM/855GME

- 200/266/333 MHz memory bus on modules with Intel® 855GME
- 200/266 MHz memory bus on modules with Intel® 852GM
- Memory: One 200-pin DDR-SO-DIMM
- 2.5V PC-1600/2100/2700 unbuffered DDR-SDRAM, up to 1GB
- Onboard video graphics array (VGA):
  Integrated in Intel® 855GME (200MHz) / 852GM (133MHz)
- Graphics memory controller hub with Intel® Extreme Graphics 2 technology
- Up to 64 MB Video RAM (UMA)
- Cathode ray tube (CRT) and low voltage differential signalling (LVDS) liquid-crystal display (LCD) interfaces

Chipset: Intel® 82801 DB (ICH4)

- Enhanced Intelligent Drive Electronics (EIDE): One Peripheral Component Interconnect (PCI) Bus Master IDE ports (up to two devices) support:
- Ultra 100/66/33 Direct Memory Access (DMA) mode
- Programmed Input/Output (PIO) modes up to Mode 4 timing
- Multiword DMA Mode with independent timing

- Universal Serial Bus (USB)
- Six USB 1.1/2.0 ports (UHCI and EHCI)
- USB legacy keyboard support
- USB floppy, CD-ROM, Hard drive, and memory stick boot support
- Integrated Ethernet: Intel 82562 10/100 Mbps Fast Ethernet controller
- Integrated, WfM 2.0 and IEEE 802.3 compliant; 10BASE-T and 100BASE-TX compatible PHY
- Audio: Integrated in Intel 82801DB southbridge
- AC97, Windows Sound System™ compatible
- NV-EEPROM for CMOS-setup retention without battery
- Real-time clock (requires external battery)

VIA VT6421 SATA Controller

- 2 Channels Serial ATA
- SATA Spec. Rev. 1.0 up to 150 MB/s per channel

BIOS

- Support for additional super I/O devices (COM1, COM2, LPT, and Floppy).
- BIOS: Phoenix, 1MB Flash-BIOS in Firmware Hub Flash Memory

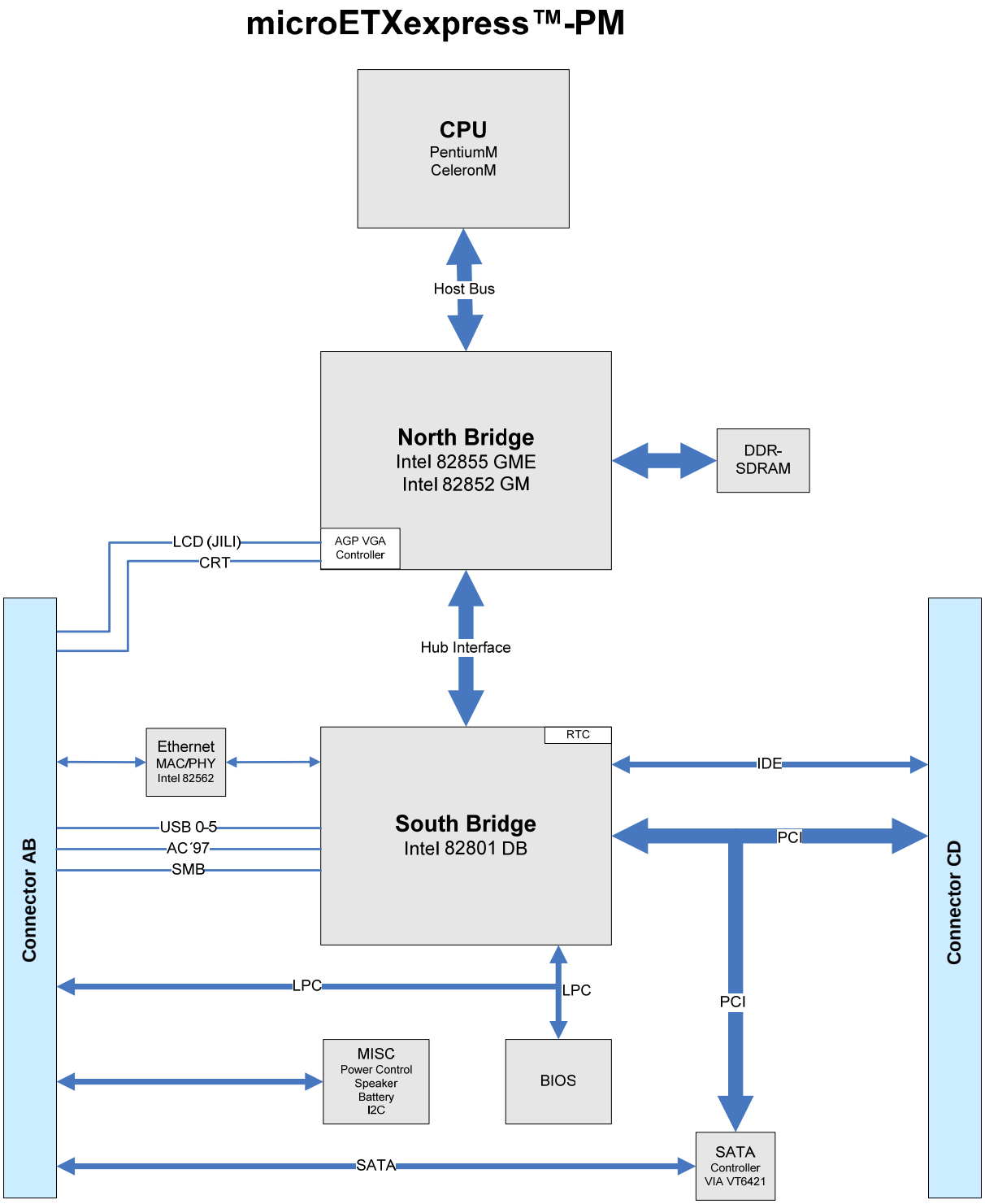
Power Management

- APM 1.2 support
- ACPI 2.0 support
- Power on Suspend (S1) and Suspend to RAM (S3) support

MARS Support

- Further details about MARS (**M**obile **A**pplication platform for **R**echargeable **S**ystems) are available at Embedded Modules Division - Kontron.

3.1.1 Block diagram



3.2 Mechanical Specifications

3.2.1 Dimensions

- 95.0 mm x 95.0 mm (3.75" x 3.75")
- Height approx. 12 mm (0.4")

3.3 Electrical Specifications

3.3.1 Supply Voltage

- 8,5 V min. - 18 V max. (ripple frequency < 10 kHz)

3.3.2 Supply Current (typical, DOS prompt)

Power-consumption tests were executed during the DOS prompt. The tested boards were mounted on a Kontron Evaluation Board (Article number: 38100-0000-00-0), a USB-mouse and a USB-keyboard were connected.

The measurements were done on the baseboard that only the corresponding current to the microETXxpress™ modul was recorded. The power consumption from devices on the Kontron Evaluation Board or connected to the Kontron Evaluation Board (for example USB-sticks, Hard drives) are not included in the measurements.

All boards were equipped with 512MB DDR SDRAM. Modules were tested using maximum CPU frequency.

CPU	DOS								
	Prompt			Standby			Suspend		
	[A]12V	[A]$5V_{SB}$	[W]	[A]12V	[A]$5V_{SB}$	[W]	[A]12V	[A]$5V_{SB}$	[W]
1400 MHz	1,15	0,22	14,90	0,72	0,22	9,74	0,72	0,22	9,74
1000 MHz	1,03	0,22	13,51	0,65	0,22	8,97	0,66	0,22	8,99
800 MHz n.c.	0,89	0,26	11,98	0,62	0,26	8,73	0,62	0,26	8,74

3.3.3 Supply Current (Windows XP SP2)

The tested boards were mounted on a Kontron Evaluation Board (Article number: 38100-0000-00-0), a USB-mouse and a USB-keyboard were connected.

The measurements were done on the baseboard that only the corresponding current to the microETXxpress™ modul was recorded. The power consumption from devices on the Kontron Evaluation Board or connected to the Kontron Evaluation Board (for example USB-sticks, Hard drives) are not included in the measurements.

The Power-consumption tests were executed during Windows XP SP2 by using a tool to stress the CPU (100 % load). The power measurements values were acquired after 15 min full load and a stable CPU die temperature. To ensure a stable die temperature a corresponding heat sink was used to hold the temperature under the critical trip point.

All boards were equipped with 512MB DDR SDRAM. The Modules were tested using maximum CPU frequency.

CPU	Windows XP										
	Standby S1			Standby S3 cold			Standby S3 hot			ACPI S5	
	[A]12V	[A]$5V_{SB}$	[W]	[A]12V	[A]$5V_{SB}$	[W]	[A]12V	[A]$5V_{SB}$	[W]	[A]$5V_{SB}$	[W]
1400 MHz	0,49	0,13	6,53	0,00	0,70	3,52	0,02	0,65	3,46	0,22	1,10
1000 MHz	0,49	0,14	6,57	0,00	0,69	3,46	0,02	0,65	3,42	0,22	1,10
800 MHz n.c.	0,49	0,13	6,55	0,00	0,70	3,52	0,01	0,66	3,45	0,25	1,25

CPU	Windows XP					
	Full Load			Idle		
	[A]12V	[A]$5V_{SB}$	[W]	[A]12V	[A]$5V_{SB}$	[W]
1400 MHz	1,62	0,22	20,54	0,78	0,22	10,46
1000 MHz	1,07	0,22	13,94	0,68	0,22	9,26
800 MHz n.c.	0,99	0,23	13,03	0,68	0,23	9,32

Note: It is difficult to test for all possible applications on the market. There may be an application that draws more power from the CPU than the measured values in the table above. This should be taken into consideration if you are on the board of the thermal specification. If this is the case improvements to your thermal solution are recommended.

3.3.4 CMOS Battery Power Consumption

RTC	Voltage Range	Quiescent Current
Integrated in the southbridge	2.0 V – 3.6 V	3.52 µA @ 3.14 V

CMOS battery power consumption was measured with a microETXexpress™-PM module on a standard Kontron ETXexpress® evaluation board. The system was turned off and the battery was removed from the evaluation board. The 2.5 V or 3.0 V of power was supplied from a DC power supply. Do not use these values to calculate the CMOS battery lifetime.

3.4 Environmental Specifications

3.4.1 Temperature

Operating: (with Kontron Embedded Modules GmbH heat-spreader plate assembly):

- Ambient temperature: 0 to +60 °C (*) without SATA controller
- Maximum heat spreader-plate temperature: 0 to +60 °C (*) (**) without SATA controller
- Non-operating: -30 to +85 °C

See the Thermal Management chapter for additional information.

Notes: **For microETXexpress™-PM modules with SATA-controller (standard) the max. temperature is reduced to 50 °C! If the SATA controller is not used and disabled in the BIOS Setup the max. temperature is 60 °C!*
***The maximum operating temperature with the heat spreader plate is the maximum measurable temperature on any spot on the heat spreader's surface. You must maintain the temperature according to the above specification.*

Operating (without Kontron Embedded Modules GmbH heat-spreader plate assembly):

- Maximum operating temperature: 0 to + 60 °C (*) (**) without SATA controller
- Maximum operating temperature: 0 to +60 °C (*) (**) without SATA controller
- Non operating: -30 to +85 °C

See the Thermal Management chapter for additional information.

Note **For microETXexpress™-PM modules with SATA-controller (standard) the max. temperature is reduced to 50 °C! If the SATA controller is not used and disabled in the BIOS Setup the max. temperature is 60 °C!*
***The maximum operating temperature is the maximum measurable temperature on any spot on a module's surface. You must maintain the temperature according to the above specification.*

3.4.2 Humidity

- Operating: 10% to 90% (non condensing)
- Non operating: 5% to 95% (non condensing)

3.5 MTBF

The following MTBF (Mean Time Between Failure) values were calculated using a combination of manufacturer's test data, if the data was available, and a Bellcore calculation for the remaining parts. The Bellcore calculation used is "Method 1 Case 1". In that particular method the components are assumed to be operating at a 50 % stress level in a 40° C ambient environment and the system is assumed to have not been burned in. Manufacturer's data has been used wherever possible. The manufacturer's data, when used, is specified at 50° C, so in that sense the following results are slightly conservative. The MTBF values shown below are for a 40° C in an office or telecommunications environment. Higher temperatures and other environmental stresses (extreme altitude, vibration, salt water exposure, etc.) lower MTBF values.

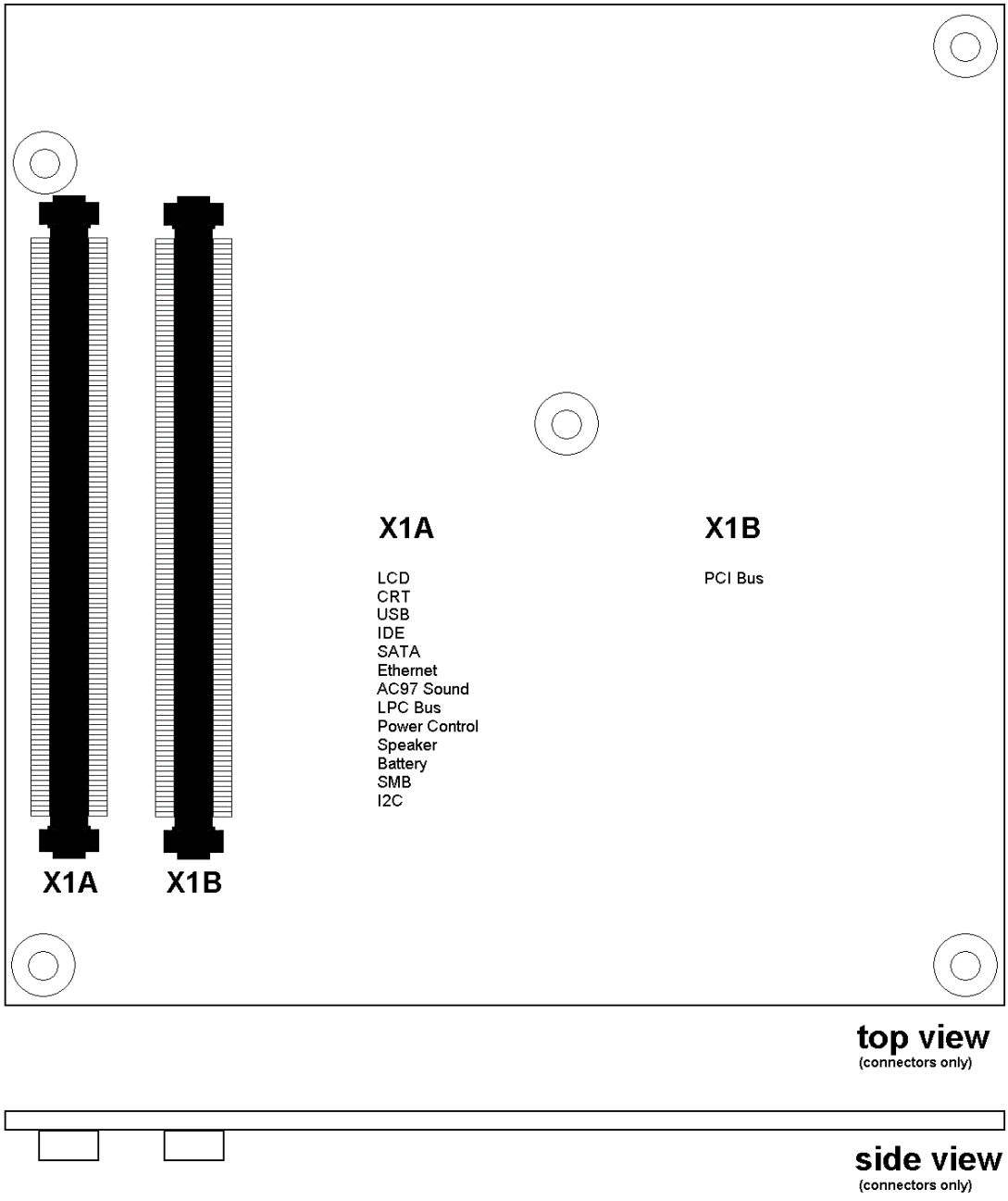
- **System MTBF (hours) : 181284**

Notes: *Fans usually shipped with Kontron Embedded Modules GmbH products have 50,000-hour typical operating life. The above estimates assume no fan, but a passive heat sinking arrangement. Estimated RTC battery life (as opposed to battery failures) is not accounted for in the above figures and need to be considered for separately. Battery life depends on both temperature and operating conditions. When the Kontron unit has external power, the only battery drain is from leakage paths.*

4 microETXexpress™-PM Connectors

The pinouts for ETXexpress® Interface Connectors X1A and X1B are documented for convenient reference. Please see the ETXexpress® Specification and ETXexpress® Design Guide for detailed, design-level information.

4.1 Connector Locations



4.2 General Signal Description

Term	Description
I	Differential Pair Input
O	Differential Pair Output
DP	Differential Pair Input/Output
OA	Output Analog
IO-3,3	Bi-directional 3,3 V IO-Signal
IO-5	Bi-directional 5 V IO-Signal
I-2,5	2,5 V Output
I-3,3	3,3 V Input
I-5	5 V Input
O-3,3	3,3 V Output
O-5	5 V Output
PU	Pull-Up Resistor
PD	Pull-Down Resistor
PWR	Power Connection
Nc	Not Connected / Reserved

4.3 Connector X1A

4.3.1 Connector X1A (Signal Levels A1-A55)

Pin A1-A55: [LAN | Power | USB | SATA | AUDIO]

Pin	Signal	Description	Type	Termination	Comment
A1	GND	Power Ground	PWR	-	-
A2	GBE0_MDI3-	n.c.	nc	-	-
A3	GBE0_MDI3+	n.c.	nc	-	-
A4	GBE0_LINK100#	LAN_SPDLED# | Ethernet Speed LED	O-3,3	-	on at 100Mb/s
A5	GBE0_LINK1000#	n.c.	nc	-	-
A6	GBE0_MDI2-	n.c.	nc	-	-
A7	GBE0_MDI2+	n.c.	nc	-	-
A8	GBE0_LINK#	LAN_LILED# | LAN Link LED	O-3,3	-	-
A9	GBE0_MDI1-	LAN_RXD- | Ethernet Receive Data -	I	-	121R between RXD+/-
A10	GBE0_MDI1+	LAN_RXD+ | Ethernet Receive Data +	I	-	121R between RXD+/-
A11	GND	Power Ground	PWR	-	-
A12	GBE0_MDI0-	LAN_TXD- | Ethernet Transmit Data -	O	-	100R/C10p between TXD+/-
A13	GBE0_MDI0+	LAN_TXD+ | Ethernet Transmit Data +	O	-	100R/C10p between TXD+/-
A14	GBE0_CTREF	ETH_CTREF	O-3,3	-	-
A15	SUS_S3#	PM_SLP_S#3_CPLD	O-3,3	-	-
A16	SATA0_TX+	SATA0_TX+ | SATA 0 Transmit Data +	O	-	-
A17	SATA0_TX-	SATA0_TX- | SATA 0 Transmit Data -	O	-	-
A18	SUS_S4#	PM_SLP_S#4_CPLD	O-3,3	-	-
A19	SATA0_RX+	SATA0_RX+ | SATA 0 Receive Data +	I	-	-
A20	SATA0_RX-	SATA0_RX- | SATA 0 Receive Data -	I	-	-
A21	GND	Power Ground	PWR	-	-
A22	SATA2_TX+	n.c.	nc	-	-
A23	SATA2_TX-	n.c.	nc	-	-
A24	SUS_S5#	PM_SLP_S#5_CPLD	O-5	PU 10k 5VSB	-
A25	SATA2_RX+	n.c.	nc	-	-
A26	SATA2_RX-	n.c.	nc	-	-
A27	BATLOW#	PM_BATLOW# | Battery Low	I-3,3	PU 10k 3,3V	-
A28	ATA_ACT#	ATA_ACT# | SATA LED	O-3,3	PU 10k 3,3V	-
A29	AC_SYNC	AC_SYNC | AC'97 Sync	O-3.3	-	int. PD 20k in ICH4
A30	AC_RST#	AC_RST# | AC'97 Reset	O-3,3	-	int. PD 20k in ICH4
A31	GND	Power Ground	PWR	-	-
A32	AC_BITCLK	AC_BITCLK | AC'97 Clock	I-3,3	-	int. PD 20k in ICH4
A33	AC_SDOUT	AC_SDATAOUT | AC'97 Data	O-3,3	-	int. PD 20k in ICH4
A34	BIOS_DISABLE#	BIOS_DISABLE#	I-3,3	-	-
A35	THRMTRIP#	PM_THRMTRIP#_CON	O-3.3	-	56R2 Ohm Resistors
A36	USB6-	n.c.	nc	-	-
A37	USB6+	n.c.	nc	-	-
A38	USB_6_7_OC#	n.c.	nc	-	-
A39	USB4-	USB_PN4 | USB Data- Port4	DP	-	int. PD 15k in ICH4
A40	USB4+	USB_PP4 | USB Data+ Port4	DP	-	int. PD 15k in ICH4
A41	GND	Power Ground	PWR	-	-
A42	USB2-	USB_PN2 | USB Data- Port2	DP	-	int. PD 15k in ICH4
A43	USB2+	USB_PP2 | USB Data+ Port2	DP	-	int. PD 15k in ICH4
A44	USB_2_3_OC#	USB_OC#_2_3 | USB OverCurrent Port 2/3	I-3,3	PU 10k 3,3V	-
A45	USB0-	USB_PN0 | USB Data- Port0	DP	-	int. PD 15k in ICH4
A46	USB0+	USB_PP0 | USB Data+ Port0	DP	-	int. PD 15k in ICH4
A47	VCC_RTC	+V_BAT	PWR	-	-
A48	EXCD0_PERST#	n.c.	nc	-	-

Pin	Signal	Description	Type	Termination	Comment
A49	EXCD0_CPPE#	n.c.	nc	-	-
A50	LPC_SERIRQ	INT_SERIRQ | Serial Interrupt Request	IO-3.3	PU 8k2 3,3V	-
A51	GND	Power Ground	PWR	-	-
A52	PCIE_TX5+	n.c.	nc	-	-
A53	PCIE_TX5-	n.c.	nc	-	-
A54	GPI0	GPI0 | General Purpose Input 0	I-3.3	PU 10k 3,3V	-
A55	PCIE_TX4+	n.c.	nc	-	-

Notes: ** To protect external power lines of peripheral devices, make sure that:*
- the wires have the right diameter to withstand the maximum available current
- the enclosure of the peripheral device fulfils the fire-protection requirements of IEC/EN60950

4.3.2 Connector X1A (Signal Levels A56-A110)

Pin A56-A110: [Power | LVDS]

Pin	Signal	Description	Type	Termination	Comment
A56	PCIE_TX4-	n.c.	nc	-	-
A57	GND	Power Ground	PWR	-	-
A58	PCIE_TX3+	n.c.	nc	-	-
A59	PCIE_TX3-	n.c.	nc	-	-
A60	GND	Power Ground	PWR	-	-
A61	PCIE_TX2+	n.c.	nc	-	-
A62	PCIE_TX2-	n.c.	nc	-	-
A63	GPI1	GPI1 | General Purpose Input 1	I-3,3	PU 10k 3,3V	-
A64	PCIE_TX1+	n.c.	nc	-	-
A65	PCIE_TX1-	n.c.	nc	-	-
A66	GND	Power Ground	PWR	-	-
A67	GPI2	GPI2 | General Purpose Input 2	I-3,3	PU 10k 3,3V	-
A68	PCIE_TX0+	n.c.	nc	-	-
A69	PCIE_TX0-	n.c.	nc	-	-
A70	GND	Power Ground	PWR	-	-
A71	LVDS_A0+	LVDS_YAP0 | LVDS Channel A Data0+	O	-	-
A72	LVDS_A0-	LVDS_YAM0 | LVDS Channel A Data0-	O	-	-
A73	LVDS_A1+	LVDS_YAP1 | LVDS Channel A Data1+	O	-	-
A74	LVDS_A1-	LVDS_YAM1 | LVDS Channel A Data1-	O	-	-
A75	LVDS_A2+	LVDS_YAP2 | LVDS Channel A Data2+	O	-	-
A76	LVDS_A2-	LVDS_YAM2 | LVDS Channel A Data2 -	O	-	-
A77	LVDS_VDD_EN	LVDS_VDDEN | LVDS Panel Power Control	O-2,5	-	int. PD 100k in 855GME
A78	LVDS_A3+	LVDS_YAP3 | LVDS Channel A Data3+	O	-	-
A79	LVDS_A3-	LVDS_YAM3 | LVDS Channel A Data3-	O	-	-
A80	GND	Power Ground	PWR	-	-
A81	LVDS_A_CK+	LVDS_CLKAP | LVDS Channel A Clock+	O	-	-
A82	LVDS_A_CK-	LVDS_CLKAM | LVDS Channel A Clock-	O	-	-
A83	LVDS_I2C_CK	LVDS_DDCPCLK | JILI I2C Clock	IO-3.3	PU 4k7 3,3V	-
A84	LVDS_I2C_DAT	LVDS_DDCPDATA | JILI I2C Data	IO-3.3	PU 4k7 3,3V	-
A85	GPI3	GPI3 | General Purpose Input 3	I-3,3	PU 10k 3,3V	-
A86	KBD_RST#	H_RCIN# | Keyboard Reset	I-3,3	-	-
A87	KBD_A20GATE	H_A20GATE	I-3,3	PU 10k 3,3V	-
A88	PCIE0_CK_REF+	n.c.	-	-	-
A89	PCIE0_CK_REF-	n.c.	-	-	-
A90	GND	Power Ground	PWR	-	-
A91	RSVD	n.c.	nc	-	-
A92	RSVD	n.c.	nc	-	-
A93	GPO0	GPO0 | General Purpose Output 0	O-3,3	PD 10k	-
A94	RSVD	n.c.	nc	-	-
A95	RSVD	n.c.	nc	-	
A96	GND	Power Ground	PWR	-	-
A97	VCC_12V	12V VCC	PWR	-	-
A98	VCC_12V	12V VCC	PWR	-	-
A99	VCC_12V	12V VCC	PWR	-	-
A100	GND	Power Ground	PWR	-	-
A101	VCC_12V	12V VCC	PWR	-	-
A102	VCC_12V	12V VCC	PWR	-	-
A103	VCC_12V	12V VCC	PWR	-	-
A104	VCC_12V	12V VCC	PWR	-	-
A105	VCC_12V	12V VCC	PWR	-	-
A106	VCC_12V	12V VCC	PWR	-	-

Pin	Signal	Description	Type	Termination	Comment
A107	VCC_12V	12V VCC	PWR	-	-
A108	VCC_12V	12V VCC	PWR	-	-
A109	VCC_12V	12V VCC	PWR	-	-
A110	GND	Power Ground	PWR	-	-

Note: The termination resistors in this table are already mounted on the microETXexpress™ board. Please refer to the ETXexpress® design guide for information about additional termination resistors.

4.4 Connector X1A (Signal Levels B1-B55)

Pin B1-B55: [LAN | Power | USB | SATA | AUDIO | LPC]

Pin	Signal	Description	Type	Termination	Comment
B1	GND	Power Ground	PWR	-	-
B2	GBE0_ACT	LAN_ACTLED# | Ethernet Activity LED	O-3,3	-	-
B3	LPC_FRAME#	LPC_FRAME# | LPC Frame Indicator	I-3,3	-	-
B4	LPC_AD0	LPC_AD0 | LPC Adress & DATA Bus	IO-3,3	-	-
B5	LPC_AD1	LPC_AD1 | LPC Adress & DATA Bus	IO-3,3	-	-
B6	LPC_AD2	LPC_AD2 | LPC Adress & DATA Bus	IO-3,3	-	-
B7	LPC_AD3	LPC_AD3 | LPC Adress & DATA Bus	IO-3,3	-	-
B8	LPC_DRQ0#	SIO_DRQ#0 | LPC Request 0	I-3,3	-	int. PU 20k 3,3V in ICH4
B9	LPC_DRQ1#	SIO_DRQ#1 | LPC Request 1	I-3,3	-	int. PU 20k 3,3V in ICH4
B10	LPC_CLK	CLK_SIOEXTPCI	O-3,3	-	33R2 in Series
B11	GND	Power Ground	PWR	-	-
B12	PWRBTN#	Power Button	I-5	-	-
B13	SMB_CK	SMB_CLK | SMBUS Clock	IO-3,3	PU 2k2 3,3V	-
B14	SMB_DAT	SMB_DATA | SMBUS Data	IO-3,3	PU 2k2 3,3V	-
B15	SMB_ALERT#	SMB_ALERT#	IO-3,3	PU 10k 3,3V	-
B16	SATA1_TX+	SATA1_TX+	O	-	-
B17	SATA1_TX-	SATA1_TX-	O	-	-
B18	SUS_STAT#	PM_SUS_ STAT#	O-3,3	-	-
B19	SATA1_RX+	SATA1_RX+	I	-	-
B20	SATA1_RX-	SATA1_RX-	I	-	-
B21	GND	Power Ground	PWR	-	-
B22	SATA3_TX+	n.c.	nc	-	-
B23	SATA3_TX-	n.c.	nc	-	-
B24	PWR_OK	17V_8.5V_PWR_OK | Power Good	I-5	-	-
B25	SATA3_RX+	n.c.	nc	-	-
B26	SATA3_RX-	n.c.	nc	-	-
B27	WDT	WDTO_CPLD | Watch Dog Trigger	O-3,3	-	-
B28	AC_SDIN2	AC_SDATAIN2 | AC'97 Serial Input Data 2	I-3,3	-	int. PD 20k in ICH4
B29	AC_SDIN1	AC_SDATAIN1 | AC'97 Serial Input Data 1	I-3,3	-	int. PD 20k in ICH4
B30	AC_SDIN0	AC_SDATAIN0 | AC'97 Serial Input Data 0	I-3,3	-	int. PD 20k in ICH4
B31	GND	Power Ground	PWR	-	-
B32	SPKR	AC_SPKR | Speaker	O-3,3	-	int. PD 20k in ICH4
B33	I2C_CK	I2CLK	O-5	PU 2k2 5V	-
B34	I2C_DAT	I2DAT	IO-5	PU 2k2 5V	-
B35	THRM#	PM THRM# CON | Over Temperature	I-3,3	PU 8k2 3,3V	-
B36	USB7-	n.c.	nc	-	-
B37	USB7+	n.c.	nc	-	-
B38	USB_4_5_OC#	USB_OC#_4_5 | USB OverCurrent Port 4/5	I-3.3	PU 10k 3,3V	-
B39	USB5-	USB_PN5 | USB Data- Port5	DP	-	int. PD 15k in ICH4
B40	USB5+	USB_PP5 | USB Data+ Port5	DP	-	int. PD 15k in ICH4
B41	GND	Power Ground	PWR	-	-
B42	USB3-	USB_PN3 | USB Data- Port3	DP	-	int. PD 15k in ICH4
B43	USB3+	USB_PP3 | USB Data+ Port3	DP	-	int. PD 15k in ICH4
B44	USB_0_1_OC#	USB_OC#_0_1 | USB OverCurrent Port 0/1	I-3.3	PU 10k 3,3V	-
B45	USB1-	USB_PN1 | USB Data- Port1	DP	-	int. PD 15k in ICH4
B46	USB1+	USB_PP1 | USB Data+ Port1	DP	-	int. PD 15k in ICH4
B47	EXCD1_PERST#	n.c.	nc	-	-
B48	EXCD1_CPPE#	n.c.	nc	-	-
B49	SYS_RESET#	RESIN# | Reset Input	I-3,3	-	-
B50	CB_RESET#	CB RESET# | PCI Bus Reset	O-3,3	-	-
B51	GND	Power Ground	PWR	-	-
B52	PCIE_RX5+	n.c.	nc	-	-

Pin	Signal	Description	Type	Termination	Comment
B53	PCIE_RX5-	n.c.	nc	-	-
B54	GPO1	GPO1 | General Purpose Output 1	O-3,3	PD 10k	-
B55	PCIE_RX4+	n.c.	nc	-	-

Note: The termination resistors in this table are already mounted on the microETXexpress™ board. Please refer to the ETXexpress® design guide for information about additional termination resistors.

4.4.1 Connector X1A (Signal Levels B56-B110)

Pin B56-B110: [Power | PCIe | LVDS | CRT]

Pin	Signal	Description	Type	Termination	Comment
B56	PCIE_RX4-	n.c.	nc	-	-
B57	GPO2	GPO2 | General Purpose Output 2	O-3,3	PD 10k	-
B58	PCIE_RX3+	n.c.	nc	-	-
B59	PCIE_RX3-	n.c.	nc	-	-
B60	GND	Power Ground	PWR	-	-
B61	PCIE_RX2+	n.c.	nc	-	-
B62	PCIE_RX2-	n.c.	nc	-	-
B63	GPO3	GPO3 | General Purpose Output 3	O-3,3	PD 10k	-
B64	PCIE_RX1+	n.c.	nc	-	-
B65	PCIE_RX1-	n.c.	nc	-	-
B66	WAKE0#	EXTSMI#	I-3,3	PU 10k 3,3V	-
B67	WAKE1#	PM_RI#	I-3,3	PU 10k 3,3V	-
B68	PCIE_RX0+	n.c.	nc	-	-
B69	PCIE_RX0-	n.c.	nc	-	-
B70	GND	Power Ground	PWR	-	-
B71	LVDS_B0+	LVDS_YBP0 | LVDS Channel B Data0+	O	-	-
B72	LVDS_B0-	LVDS_YBM0 | LVDS Channel B Data0-	O	-	-
B73	LVDS_B1+	LVDS_YBP1 | LVDS Channel B Data1+	O	-	-
B74	LVDS_B1-	LVDS_YBM1 | LVDS Channel B Data1-	O	-	-
B75	LVDS_B2+	LVDS_YBP2 | LVDS Channel B Data2+	O	-	-
B76	LVDS_B2-	LVDS_YBM2 | LVDS Channel B Data2 -	O	-	-
B77	LVDS_B3+	LVDS_YBP2 | LVDS Channel B Data3+	O	-	-
B78	LVDS_B3-	LVDS_YBM2 | LVDS Channel B Data3 -	O	-	-
B79	LVDS_BKLT_EN	BLON# | Panel Backlight ON	O-3,3	-	-
B80	GND	Power Ground	PWR	-	-
B81	LVDS_B_CK+	LVDS_CLKBP | LVDS Channel B Clock+	O	-	-
B82	LVDS_B_CK-	LVDS_CLKBM | LVDS Channel B Clock-	O	-	-
B83	LVDS_BKLT_CTRL	LVDS BKLTCTL | Backlight Brightness Contr.	O	-	int. PD 100k in 855GME
B84	VCC_5V_SBY	+V_STBY_ETX | 5V Standby	PWR	-	-
B85	VCC_5V_SBY	+V_STBY_ETX | 5V Standby	PWR	-	-
B86	VCC_5V_SBY	+V_STBY_ETX | 5V Standby	PWR	-	-
B87	VCC_5V_SBY	+V_STBY_ETX | 5V Standby	PWR	-	-
B88	RSVD	n.c.	nc	-	-
B89	VGA_RED	DAC_RED | Analog Video RGB-RED	O	-	-
B90	GND	Power Ground	PWR	-	-
B91	VGA_GRN	DAC_GREEN | Analog Video RGB-GREEN	O	-	-
B92	VGA_BLU	DAC_BLUE | Analog Video RGB-BLUE	O	-	-
B93	VGA_HSYNC	DAC_HSYNC | Analog Video H-Sync	O-3,3	-	-
B94	VGA_VSYNC	DAC_VSYNC | Analog Video V-Sync	O-3,3	-	-
B95	VGA_I2C_CK	DAC_DDCACLK | Display Data Channel Clock	IO-5	PU 4k7 5V	-
B96	VGA_I2C_DAT	DAC_DDCADATA | Display Data Channel Data	IO-5	PU 4k7 5V	-
B97	TV_DAC_A	n.c.	nc	-	-
B98	TV_DAC_B	n.c.	nc	-	-
B99	TV_DAC_C	n.c.	nc	-	-
B100	GND	Power Ground	PWR	-	-
B101	VCC_12V	12V VCC	PWR	-	-
B102	VCC_12V	12V VCC	PWR	-	-
B103	VCC_12V	12V VCC	PWR	-	-
B104	VCC_12V	12V VCC	PWR	-	-
B105	VCC_12V	12V VCC	PWR	-	-
B106	VCC_12V	12V VCC	PWR	-	-
B107	VCC_12V	12V VCC	PWR	-	-

Pin	Signal	Description	Type	Termination	Comment
B108	VCC_12V	12V VCC	PWR	-	-
B109	VCC_12V	12V VCC	PWR	-	-
B110	GND	Power Ground	PWR	-	-

4.4.2 Connector X1A Subsystems

Ethernet

The Ethernet interface is based on the Intel® 82562 Fast Ethernet PCI controller. This 32-bit PCI controller is a fully integrated 10/100BASE-TX LAN solution.

The Ethernet interface requires an external transformer. See the *ETXexpress® Design Guide* for suggestions on transformer selection.

Configuration

The Ethernet interface is a PCI device. The BIOS setup automatically configures it during configuration of the PCI device.

Note: *Implementation and limitation information is provided in the ETXexpress® Design Guide. Refer to the documentation for additional information.*

Serial IRQ

The serial IRQ pin offers a standardized interface to link interrupt request lines to a single wire.

Configuration

The serial IRQ machine is in “Quiet Mode”, the frame size is 21 frames and the frame pulse width is 4 clocks.

USB

Three USB host controllers (two 1.1 UHCI and one EHCI high-speed 2.0 controller) are on the Intel® 82801DB south bridge device. The USB controllers comply with both versions 1.1 and 2.0 of the USB standard and are backward compatible. The three controllers implement a root hub, which have two USB ports each.

Configuration

The USB controllers are PCI bus devices. The BIOS allocates required system resources during configuration of the PCI bus.

SATA

The VIA VT6421 SATA Controller offers the possibility to connect 2 SATA Hard disks according SATA Specification 1.0 with 150 MB/s per channel.

Configuration

The SATA controller is a PCI bus device. The BIOS allocates required system resources during configuration of the PCI bus.

Audio

The micro*ETXexpress™-PM* PCI audio controller is integrated in the Intel® 82801DB Southbridge.

Configuration

The audio controller is a PCI bus device. The BIOS allocates required system resources during configuration of the PCI device.

VGA Output

The micro*ETXexpress™-PM* graphics subsystem is integrated in the Intel® 852GM/855GME northbridge. It has the following features:

- Display image rotation
- Display core frequency at 133 MHz (852GM); 200 MHz or 250 MHz (855GME)
- Render core frequency at 133 MHz (852GM); 100 MHz, 133 MHz, 166 MHz, 200 MHz, 250 MHz (855GME)
- 2D graphics engine
- Improved hardware motion compensation for MPEG2
- Software DVD at 60 Fields/second and 30 frames/second full screen
- Support for standard definition DVD (i.e. NTSC pixel resolution of 720x480, etc.) quality encoding at low CPU utilization
- Single- or dual-channel LVDS panel support up to UXGA panel resolution with frequency range from 25 MHz to 112 MHz (single channel/dual channel)
- 3D graphics engine
- 3D setup and render engine
- Zone rendering
- High quality performance texture engine
- Viewpoint transform and perspective divide
- It can drive cathode ray tube (CRT) monitors and flat-panel displays, using the JUMPtec Intelligent LVDS Interface (JILI). You can program the graphics controller to use up the 32MB of unified memory architecture (UMA) memory as its video memory.
- Max. resolution CRT: 2048x1536 at 75 Hz (855GME), 1920x1440 at 60 Hz (852GM)
- Max. resolution LCD: UXGA 1600x1200 (4G colors); Bits/Pixels supported 1x18 bit, 2x18 bit, 1x24 bit*, 2x24 bit*

*Note: *The 852GM/855GME does not support 24 bit LVDS but emulates the missing 2 bits per color and most of the panels can be used with this limitation.*

Configuration

The graphics controller requires the following resources:

- An IRQ
- Several I/O addresses

- Memory-address blocks in high memory

The BIOS allocates the resources during AGP configuration. Many resources are set for compatibility with industry-standard settings.

LVDS Flat Panel Interface (JILI)

The user interface for flat panels is the JUMPtec Intelligent LVDS Interface (JILI). The implementation of this subsystem complies with the *ETXexpress® Specification*. Implementation information is provided in the *ETXexpress® Design Guide*. Refer to the documentation for additional information.

Digital Flat Panel Interface (JIDI)

The micro*ETXexpress™-PM* does not support the JUMPtec Intelligent Digital Interface (JIDI).

Power Control

Power Good / Reset Input

The micro*ETXexpress™-PM* provides an external input for a power-good signal or a manual- reset pushbutton. The implementation of this subsystem complies with the *ETXexpress® Specification*. Implementation information is provided in the *ETXexpress® Design Guide*. Refer to the documentation for additional information.

Power Management

ATX PS Control

The micro*ETXexpress™-PM* can control the main power output of an ATX-style power supply. The implementation of this subsystem complies with the *ETXexpress® Specification*. Implementation information is provided in the *ETXexpress® Design Guide*. Refer to the documentation for additional information.

External SMI Interrupt

Contact Kontron Embedded Modules technical support for information on this feature.

Speaker

The implementation of the speaker output complies with the *ETXexpress® Specification*. Implementation information is provided in the *ETXexpress® Design Guide*. Refer to the documentation for additional information.

Battery

The implementation of the battery input complies with the *ETXexpress® Specification*. Implementation information is provided in the *ETXexpress® Design Guide*. Refer to the documentation for additional information.

In compliance with EN60950, there are at least two current-limiting devices (resistor and diode) between the battery and the consuming component.

I²C Bus

The I²C Bus is implemented by using general purpose I/O.

You also can access the I²C Bus via JUMP*tec*'s Intelligent Device Architecture (JIDA) BIOS functions.

For additional information, refer to the *ETXexpress® Design Guide*, I²C application notes and JIDA specifications which are available at the Kontron Web site.

SM Bus

System Management (SM) bus signals are connected to the SM bus controller, which is located in the Southbridge (Intel 82801DB) device. For more information about the SM bus, please see the System Management (SM) Bus section in the System Resources chapter.

LPC Bus

The Low Pin Count Interface signals are connected to the LPC Bus controller, which is located in the Winbond Super I/O Controller. The LPC low speed interface can be used for peripheral circuits such as an external Super I/O Controller, which typically combine legacy-device support into a single IC. The implementation of this subsystem complies with the *ETXexpress® Specification*. Implementation information is provided in the *ETXexpress® Design Guide*. Refer to the documentation for additional information.

4.5 Connector X1B

4.5.1 Connector X1B (Signal Levels C1-C55)

Pin C1-C55: [IDE | Power | PCI | | PEG]

Pin	Signal	Description	Type	Termination	Comment
C1	GND	Power Ground	PWR	-	-
C2	IDE_D7	IDE Data Bus	IO	-	-
C3	IDE_D6	IDE Data Bus	IO	-	-
C4	IDE_D3	IDE Data Bus	IO	-	-
C5	IDE_D15	IDE Data Bus	IO	-	-
C6	IDE_D8	IDE Data Bus	IO	-	-
C7	IDE_D9	IDE Data Bus	IO	-	-
C8	IDE_D2	IDE Data Bus	IO	-	-
C9	IDE_D13	IDE Data Bus	IO	-	-
C10	IDE_D1	IDE Data Bus	IO	-	-
C11	GND	Power Ground	PWR	-	-
C12	IDE_D14	IDE Data Bus	IO	-	-
C13	IDE_IORDY	IDE Ready	I-3,3	PU 1k1 3,3V	-
C14	IDE_IOR#	IDE IO Read	O-3,3	-	-
C15	PCI_PME#	PCI Power Management Event	IO-3,3	-	-
C16	PCI_GNT2#	PCI Bus Grant 2	O-3,3	-	-
C17	PCI_REQ2#	PCI Bus Request 2	I-3,3	PU 8k2 3,3V	-
C18	PCI_GNT1#	PCI Bus Grant 1	O-3,3		-
C19	PCI_REQ1#	PCI Bus Request 1	I-3,3	PU 8k2 3,3V	-
C20	PCI_GNT0#	PCI Bus Grant 0	O-3,3		-
C21	GND	Power Ground	PWR	-	-
C22	PCI_REQ0#	PCI Bus Reqest 0	I-3,3	PU 8k2 3,3V	-
C23	PCI_RESET#	PCI Bus Reset	O-3,3	-	-
C24	PCI_AD0	PCI Adress & Data Bus line	IO-3,3	-	-
C25	PCI_AD2	PCI Adress & Data Bus line	IO-3,3	-	-
C26	PCI_AD4	PCI Adress & Data Bus line	IO-3,3	-	-
C27	PCI_AD6	PCI Adress & Data Bus line	IO-3,3	-	-
C28	PCI_AD8	PCI Adress & Data Bus line	IO-3,3	-	-
C29	PCI_AD10	PCI Adress & Data Bus line	IO-3,3	-	-
C30	PCI_AD12	PCI Adress & Data Bus line	IO-3,3	-	-
C31	GND	Power Ground	PWR	-	-
C32	PCI_AD14	PCI Adress & Data Bus line	IO-3,3	-	-
C33	PCI_C/BE1#	PCI Bus Command and Byte enables 1	IO-3,3	-	-
C34	PCI_PERR#	PCI Bus Grant Error	IO-3,3	PU 8k2 3,3V	-
C35	PCI_LOCK#	PCI Bus Lock	IO-3,3	PU 8k2 3,3V	-
C36	PCI_DEVSEL#	PCI Bus Device Select	IO-3,3	PU 8k2 3,3V	-
C37	PCI_IRDY#	PCI Bus Bus Initiator Ready	IO-3,3	PU 8k2 3,3V	-
C38	PCI_C/BE2#	PCI Bus Command and Byte enables 2	IO-3,3	-	-
C39	PCI_AD17	PCI Adress & Data Bus line	IO-3,3	-	-
C40	PCI_AD19	PCI Adress & Data Bus line	IO-3,3	-	-
C41	GND	Power Ground	PWR	-	-
C42	PCI_AD21	PCI Adress & Data Bus line	IO-3,3	-	-
C43	PCI_AD23	PCI Adress & Data Bus line	IO-3,3	-	-
C44	PCI_C/BE3#	PCI Bus Command and Byte enables 3	IO-3,3	-	-
C45	PCI_AD25	PCI Adress & Data Bus line	IO-3,3	-	-
C46	PCI_AD27	PCI Adress & Data Bus line	IO-3,3	-	-
C47	PCI_AD29	PCI Adress & Data Bus line	IO-3,3	-	-

Pin	Signal	Description	Type	Termination	Comment
C48	PCI_AD31	PCI Adress & Data Bus line	IO-3,3	-	-
C49	PCI_IRQA#	PCI Bus Interrupt Request A	I-3,3	PU 8k2 3,3V	-
C50	PCI_IRQB#	PCI Bus Interrupt Request B	I-3,3	PU 8k2 3,3V	-
C51	GND	Power Ground	PWR	-	-
C52	PEG_RX0+	n.c.	I	-	-
C53	PEG_RX0-	n.c.	I	-	-
C54	TYPE0#	n.c.	nc	-	-
C55	PEG_RX1+	n.c.	I	-	-

Note: The termination resistors in this table are already mounted on the microETXexpress™ board. Please refer to the ETXexpress® design guide for information about additional termination resistors.

4.5.2 Connector X1B (Signal Levels C56-C110)

Pin C56-C110: [Power | PCIe]

Pin	Signal	Description	Type	Termination	Comment
C56	PEG_RX1-	n.c.	nc	-	-
C57	TYPE1#	n.c.	nc	-	-
C58	PEG_RX2+	n.c.	nc	-	-
C59	PEG_RX2-	n.c.	nc	-	-
C60	GND	Power Ground	PWR	-	-
C61	PEG_RX3+	n.c.	nc	-	-
C62	PEG_RX3-	n.c.	nc	-	-
C63	RSVD	-	nc	-	-
C64	RSVD	-	nc	-	-
C65	PEG_RX4+	n.c.	nc	-	-
C66	PEG_RX4-	n.c.	nc	-	-
C67	RSVD	EXT_COM_EN#	nc	-	-
C68	PEG_RX5+	n.c.	nc	-	-
C69	PEG_RX5-	n.c.	nc	-	-
C70	GND	Power Ground	PWR	-	-
C71	PEG_RX6+	n.c.	nc	-	-
C72	PEG_RX6-	n.c.	nc	-	-
C73	SDVO_DATA	n.c.	nc	-	-
C74	PEG_RX7+	n.c.	nc	-	-
C75	PEG_RX7-	n.c.	nc	-	-
C76	GND	Power Ground	PWR	-	-
C77	RSVD	n.c.	nc	-	-
C78	PEG_RX8+	n.c.	nc	-	-
C79	PEG_RX8-	n.c.	nc	-	-
C80	GND	Power Ground	PWR	-	-
C81	PEG_RX9+	n.c.	nc	-	-
C82	PEG_RX9-	n.c.	nc	-	-
C83	RSVD	n.c.	nc	-	-
C84	GND	Power Ground	PWR	-	-
C85	PEG_RX10+	n.c.	nc	-	-
C86	PEG_RX10-	n.c.	nc	-	-
C87	GND	Power Ground	PWR	-	-
C88	PEG_RX11+	n.c.	nc	-	-
C89	PEG_RX11-	n.c.	nc	-	-
C90	GND	Power Ground	PWR	-	-
C91	PEG_RX12+	n.c.	nc	-	-
C92	PEG_RX12-	n.c.	nc	-	-
C93	GND	Power Ground	PWR	-	-
C94	PEG_RX13+	n.c.	nc	-	-
C95	PEG_RX13-	n.c.	nc	-	-
C96	GND	Power Ground	PWR	-	-
C97	RSVD	n.c.	nc	-	-
C98	PEG_RX14+	n.c.	nc	-	-
C99	PEG_RX14-	n.c.	nc	-	-
C100	GND	Power Ground	PWR	-	-
C101	PEG_RX15+	n.c.	nc	-	-
C102	PEG_RX15-	n.c.	nc	-	-
C103	GND	Power Ground	PWR	-	-
C104	VCC_12V	12V VCC	PWR	-	-
C105	VCC_12V	12V VCC	PWR	-	-
C106	VCC_12V	12V VCC	PWR	-	-
C107	VCC_12V	12V VCC	PWR	-	-

Pin	Signal	Description	Type	Termination	Comment
C108	VCC_12V	12V VCC	PWR	-	-
C109	VCC_12V	12V VCC	PWR	-	-
C110	GND	Power Ground	PWR	-	-

4.5.3 Connector X1B (Signal Levels D1-D55)

Pin D1-D55: [IDE | Power | PCI PEG]

Pin	Signal	Description	Type	Termination	Comment
D1	GND	Power Ground	PWR	-	-
D2	IDE_D5	IDE Data Bus	IO	-	-
D3	IDE_D10	IDE Data Bus	IO	-	-
D4	IDE_D11	IDE Data Bus	IO	-	-
D5	IDE_D12	IDE Data Bus	IO	-	-
D6	IDE_D4	IDE Data Bus	IO	-	-
D7	IDE_D0	IDE Data Bus	IO	-	-
D8	IDE_REQ	IDE Data Bus	IO	-	-
D9	IDE_IOW#	IDE IO Write	O-3,3	-	-
D10	IDE_ACK#	IDE DMA Acknowledge	O-3,3	-	-
D11	GND	Power Ground	PWR	-	-
D12	IDE_IRQ	IDE Interrupt Request	I-3,3	PU 8k2 3,3V	-
D13	IDE_A0	IDE Adress Bus	O-3,3	-	-
D14	IDE_A1	IDE Adress Bus	O-3,3	-	-
D15	IDE_A2	IDE Adress Bus	O-3,3	-	-
D16	IDE_CS1#	IDE Chip Select Channel 0	O-3,3	-	-
D17	IDE_CS3#	IDE Chip Select Channel 1	O-3,3	-	-
D18	IDE_RESET#	IDE Hard Drive Reset	O-3,3	-	-
D19	PCI_GNT3#	PCI Bus Grant 3	O-3,3	-	-
D20	PCI_REQ3#	PCI Bus Reqest 0	I-3,3	PU 8k2 3,3V	-
D21	GND	Power Ground	PWR	-	-
D22	PCI_AD1	PCI Adress & Data Bus line	IO-3,3	-	-
D23	PCI_AD3	PCI Adress & Data Bus line	IO-3,3	-	-
D24	PCI_AD5	PCI Adress & Data Bus line	IO-3,3	-	-
D25	PCI_AD7	PCI Adress & Data Bus line	IO-3,3	-	-
D26	PCI_C/BE0#	PCI Bus Command and Byte enables 0	IO-3,3	-	-
D27	PCI_AD9	PCI Adress & Data Bus line	IO-3,3	-	-
D28	PCI_AD11	PCI Adress & Data Bus line	IO-3,3	-	-
D29	PCI_AD13	PCI Adress & Data Bus line	IO-3,3	-	-
D30	PCI_AD15	PCI Adress & Data Bus line	IO-3,3	-	-
D31	GND	Power Ground	PWR	-	-
D32	PCI_PAR	PCI Bus Parity	IO-3,3	-	-
D33	PCI_SERR#	PCI Bus System Error	IO-3,3	PU 8k2 3,3V	-
D34	PCI_STOP#	PCI Bus Stop	IO-3,3	PU 8k2 3,3V	-
D35	PCI_TRDY#	PCI Bus Target Ready	IO-3,3	PU 8k2 3,3V	-
D36	PCI_FRAME#	PCI Bus Cycle Frame	IO-3,3	PU 8k2 3,3V	-
D37	PCI_AD16	PCI Adress & Data Bus line	IO-3,3	-	-
D38	PCI_AD18	PCI Adress & Data Bus line	IO-3,3	-	-
D39	PCI_AD20	PCI Adress & Data Bus line	IO-3,3	-	-
D40	PCI_AD22	PCI Adress & Data Bus line	IO-3,3	-	-
D41	GND	Power Ground	PWR	-	-
D42	PCI_AD24	PCI Adress & Data Bus line	IO-3,3	-	-
D43	PCI_AD26	PCI Adress & Data Bus line	IO-3,3	-	-
D44	PCI_AD28	PCI Adress & Data Bus line	IO-3,3	-	-
D45	PCI_AD30	PCI Adress & Data Bus line	IO-3,3	-	-
D46	PCI_IRQC#	PCI Bus Interrupt Request C	I-3,3	PU 8k2 3,3V	-
D47	PCI_IRQD#	PCI Bus Interrupt Request D	I-3,3	PU 8k2 3,3V	-
D48	PCI_CLKRUN#	PCI Clock Run	I-3,3	PU 10k 3,3V	-
D49	PCI_M66EN	n.c.	nc	-	-
D50	PCI_CLK	PCI Clock	O-3,3	-	-
D51	GND	Power Ground	PWR	-	-
D52	PEG_TX0+	n.c.	nc	-	-

Pin	Signal	Description	Type	Termination	Comment
D53	PEG_TX0-	n.c.	nc	-	-
D54	PEG_LANE_RV#	n.c.	nc	-	-
D55	PEG_TX1+	n.c.	nc	-	-

Note: The termination resistors in this table are already mounted on the microETXexpress™ board. Please refer to the ETXexpress® design guide for information about additional termination resistors.

4.5.4 Connector X1B (Signal Levels D56-D110)

Pin	Signal	Description	Type	Termination	Comment
D56	PEG_TX1-	n.c.	nc	-	-
D57	TYPE2#	n.c.	nc	-	-
D58	PEG_TX2+	n.c.	nc	-	-
D59	PEG_TX2-	n.c.	nc	-	-
D60	GND	Power Ground	PWR	-	-
D61	PEG_TX3+	n.c.	nc	-	-
D62	PEG_TX3-	n.c.	nc	-	-
D63	RSVD	-	nc	-	
D64	RSVD	-	nc	-	
D65	PEG_TX4+	n.c.	nc	-	-
D66	PEG_TX4-	n.c.	nc	-	-
D67	GND	Power Ground	PWR	-	-
D68	PEG_TX5+	n.c.	nc	-	-
D69	PEG_TX5-	n.c.	nc	-	-
D70	GND	Power Ground	PWR	-	-
D71	PEG_TX6+	n.c.	nc	-	-
D72	PEG_TX6-	n.c.	nc	-	-
D73	SDVO_CLK	n.c.	nc	-	-
D74	PEG_TX7+	n.c.	nc	-	-
D75	PEG_TX7-	n.c.	nc	-	-
D76	GND	Power Ground	PWR	-	-
D77	IDE_CBLID	IDE Primary ATA Detect	I-3,3	PD 10k	
D78	PEG_TX8+	n.c.	nc	-	-
D79	PEG_TX8-	n.c.	nc	-	-
D80	GND	Power Ground	PWR	-	-
D81	PEG_TX9+	n.c.	nc	-	-
D82	PEG_TX9-	n.c.	nc	-	-
D83	RSVD	n.c.	nc	-	-
D84	GND	Power Ground	PWR	-	-
D85	PEG_TX10+	n.c.	nc	-	-
D86	PEG_TX10-	n.c.	nc	-	-
D87	GND	Power Ground	PWR	-	-
D88	PEG_TX11+	n.c.	nc	-	-
D89	PEG_TX11-	n.c.	nc	-	-
D90	GND	Power Ground	PWR	-	-
D91	PEG_TX12+	n.c.	nc	-	-
D92	PEG_TX12-	n.c.	nc	-	-
D93	GND	Power Ground	PWR	-	-
D94	PEG_TX13+	n.c.	nc	-	-
D95	PEG_TX13-	n.c.	nc	-	-
D96	GND	Power Ground	PWR	-	-
D97	PEG_ENABLE#	n.c.	nc	-	-
D98	PEG_TX14+	n.c.	nc	-	-
D99	PEG_TX14-	n.c.	nc	-	-
D100	GND	Power Ground	PWR	-	-
D101	PEG_TX15+	n.c.	nc	-	-
D102	PEG_TX15-	n.c.	nc	-	-
D103	GND	Power Ground	PWR	-	-
D104	VCC_12V	12V VCC	PWR	-	-
D105	VCC_12V	12V VCC	PWR	-	-
D106	VCC_12V	12V VCC	PWR	-	-
D107	VCC_12V	12V VCC	PWR	-	-
D108	VCC_12V	12V VCC	PWR	-	-

Pin	Signal	Description	Type	Termination	Comment
D109	VCC_12V	12V VCC	PWR	-	-
D110	GND	Power Ground	PWR	-	-

Note: The termination resistors in this table are already mounted on the ETXexpress® board. Please refer to the design guide for information about additional termination resistors.

*Notes: *To protect external power lines of peripheral devices, make sure that:*
- the wires have the right diameter to withstand the maximum available current
- the enclosure of the peripheral device fulfils the fire-protection requirements of IEC/EN60950.
***This signal is not supported on the microETXexpress™-PM.*

4.5.5 Connector X1B Subsystems

PCI Bus

The implementation of this subsystem complies with the *ETXexpress® / COMexpress Specification*. Implementation information is provided in the *ETXexpress® Design Guide*. Refer to the documentation for additional information.

IDE Port

The IDE host adapter is capable of DMA-33*/66*/100* operation. The implementation of this subsystem complies with the *ETXexpress® Specification*. Implementation information is provided in the *ETXexpress® Design Guide*. Refer to those documents for additional information.

*Note: *For UDMA-100/66 operation please follow the System Guidelines for ULTRA DMA of the ATA-Specification. The ETX®-concept in combination with peripheral devices (cable, connectors, base board layout...) can worse the transmission quality so that it is necessarily to decrease the UDMA-Mode to values below 3.*

Configuration

The IDE host adapter is a PCI bus device. It is configured by the BIOS during PCI device configuration. You can disable it in setup. Resources used by the IDE host adapter are compatible with the PC/AT.

***Note:** PHOENIX BIOS will not recognize a Slave device on the IDE port if there is no Master device connected.*

5 Special Features

5.1 Watchdog Timer

You can configure the Watchdog Timer (WDT) in BIOS setup to start after a set amount of time after power-on boot. The WDT can also be controlled by the JIDA32 Library API (Refer to Appendix A: JIDA Standard). The application software should strobe the WDT to prevent its timeout. Upon timeout, the WDT resets and restarts the system. This provides a way to recover from program crashes or lockups.

Configuration

You can program the timeout period for the watchdog timer in two ranges:

- 1-second increments from 1 to 255 seconds
- 1-minute increments from 1 to 255 minutes

Contact Kontron Embedded Modules technical support for information on programming and operating the WDT.

6 Important Information

Kontron Embedded Modules GmbH currently offers different variants of the microETXexpress™-PM. They are the 1400 MHz PentiumM and the 800 MHz and 1000MHz CeleronM versions. These variants utilize a smart BIOS that is capable of identifying the CPU that the module is equipped with. Another feature of the BIOS is its ability to offer the user the option to set the maximum CPU frequency when using modules equipped with the 1400 MHz PentiumM. The Celerons 800 MHz and 1000MHz does not support this option.

6.1 Max CPU Frequency setting

The 1400MHz variant offers the option to set the maximum CPU frequency using a setting in the BIOS setup located in the Power Menu page.

The different Max CPU frequency settings available are as follows:

1400 MHz
1300 MHz
1200 MHz
1100 MHz
1000 MHz
900 MHz
800 MHz
600 MHz

6.2 Max CPU Frequency default settings

Each microETXexpress™-PM module that supports the Max CPU Frequency setting option has a predefined default frequency setting.

➤ On the 1400MHz version this default setting is 1400MHz.

6.3 Limitations

With the introduction of higher frequency CPUs new problems arise when considering cooling solutions. Although these higher frequency CPUs offer greater performance they also produce more heat, which must be efficiently dissipated from the application.

As mentioned in the previous section each microETXexpress™-PM module that supports the Max CPU Frequency setting option has a predefined default frequency setting. This is done to ensure that the module can operate using the standard microETXexpress™-PM heatspreader without reaching the “Critical Trip Point” when used at room temperature (typical 24°C).

The “Critical Trip Point” is designed to ensure that the module is shut down before any thermal damage can occur to the CPU. This feature is available on all microETXexpress™-PM modules. If the cooling

solution is unable to maintain a temperature below the "Critical Trip Point" then the module is automatically shut down. The "Critical Trip Point" feature only works in conjunction with an ATX power supply or power supplies that utilize the PS_ON signal.

Warning: AT power supplies do not support the "Critical Trip Point" feature.

6.3.1 microETXexpress™-PM Celeron 800 MHz and 1000 MHz

Kontron Embedded Modules GmbH also offers an microETXexpress™-PM Celeron 800 MHz and 1000 MHz. This module does not support the "Max CPU Frequency" setting option mentioned earlier in this section but does support the "Critical Trip Point" feature. Due to the fact that this particular CPU does not support the "Max CPU Frequency" setting option it always operates at maximum frequency and generates extreme heat. This means that this module is unable to operate using the standard microETXexpress™-PM heatspreader as its only means of thermal interface and therefore requires a special cooling solution for use. You must ensure that you design a cooling solution that will allow the excess heat to be dissipated from the application so that the "Critical Trip Point" is not reached causing the module to shut down.

Additionally the microETXexpress™-PM Celeron 800 MHz and 1000 MHz does not support INTEL speed step. As a result of this the default value for the "Automatic Thermal Monitor Control Circuit" in the BIOS setup is TM1 instead of TM2. The microETXexpress™-PM Celeron 800 MHz and 1000 MHz does not support TM2. See sections Thermal Monitor and Catastrophic Thermal Protection and Power Menu of this document for more information about TM1 and TM2.

Warning: AT power supplies do not support the "Critical Trip Point" feature.

6.4 Cooling Solutions

With introduction of higher frequency CPUs into the embedded market the need to design more efficient cooling solutions is now a necessity. These higher frequency CPUs generate much more heat, which must be removed from the application. One solution that has become more common in the embedded market is the use of heat pipes when designing a cooling solution. Kontron Embedded Modules GmbH has designed some cooling solutions that utilize heat pipes in order to perform some tests. Although Kontron Embedded Modules GmbH designed these cooling solutions strictly for test purposes, and not as a standard ETXexpress® cooling solution, the knowledge gained from these tests is being made available to customers in the form of an application note called PM_Thermal_Guidelines_E1xx.pdf. This application note should be used as a guideline to help evaluate potential thermal designs. It can be found on Kontron's web site at http://www.kontron-emea.com/emd on the ETXexpress® product page and in the Tech Support section.

7 Design Considerations

7.1 Thermal Management

A heat-spreader plate assembly is available from Kontron Embedded Modules GmbH for the microETXexpress™-PM. The heat-spreader plate on top of this assembly is NOT a heat sink. It works as an ETXexpress®-standard thermal interface to use with a heat sink or other cooling device.

External cooling must be provided to maintain the heat-spreader plate at proper operating temperatures. Under worst-case conditions, the cooling mechanism must maintain an ambient air and heat-spreader plate temperature of 60° C or less.

The aluminum slugs and thermal pads on the underside of the heat-spreader assembly implement thermal interfaces between the heat spreader plate and the major heat-generating components on the microETXexpress™-PM. About 80 percent of the power dissipated within the module is conducted to the heat-spreader plate and can be removed by the cooling solution.

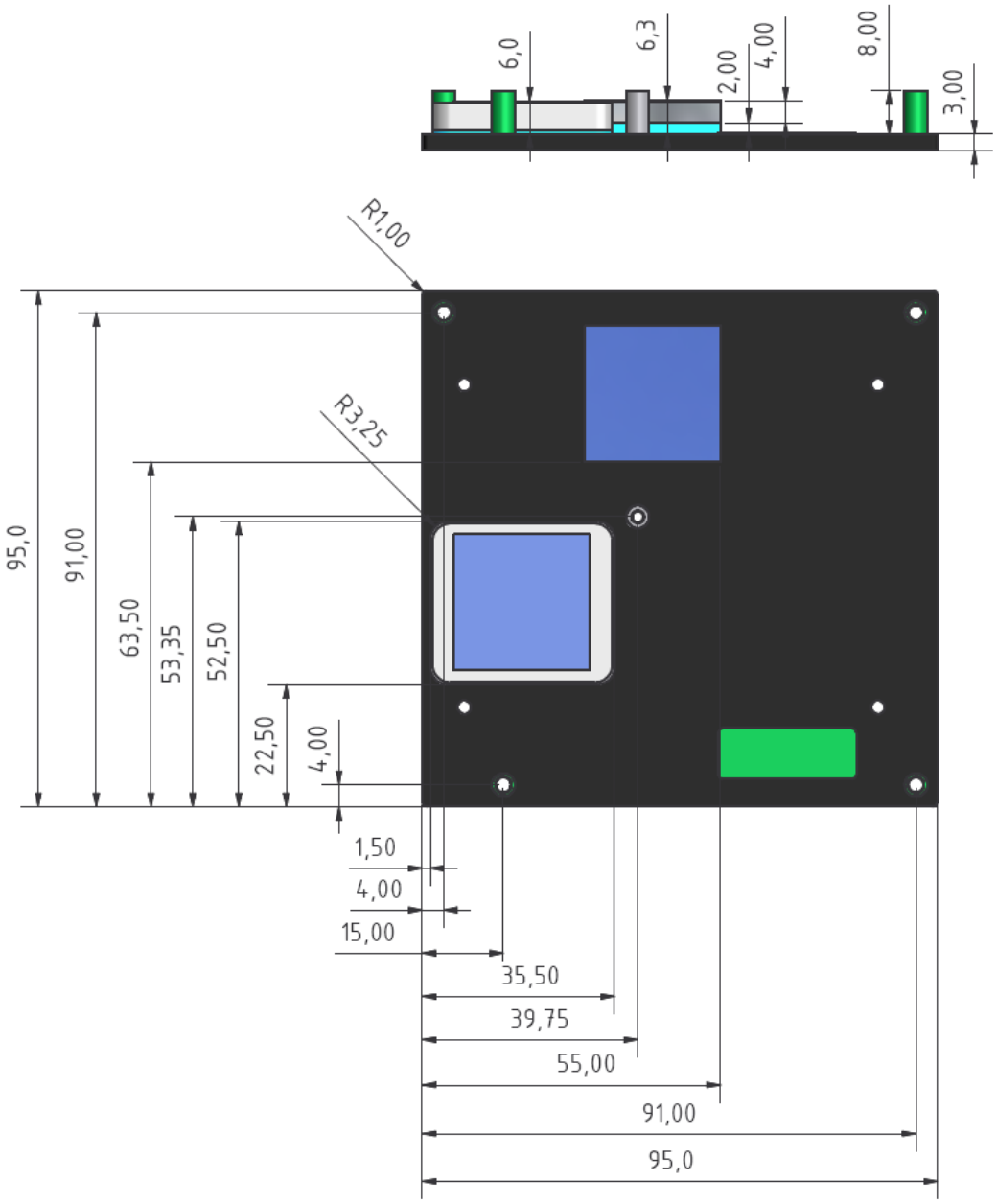
For 1400 MHz modules, the heat dissipated into the plate ranges from 18 to 20 watts. Design a cooling solution to dissipate the heat load on a heat-spreader plate at a minimum of 20 watts to accommodate all microETXexpress™-PM modules.

You can use many thermal-management solutions with the heat-spreader plates, including active and passive approaches. The optimum cooling solution varies, depending on the ETXexpress® application and environmental conditions. Please see the ETXexpress® Design Guide for further information on thermal management.

7.2 Heat spreader Dimensions

7.2.1 microETXexpress™-PM Heatspreader

This is the backside view of the heatspreader plate with pads marked for the heat generating components for microETXexpress™-PM Modules.



Article numbers:

36001-0000-99-0 HSP-PM threaded stand off

36001-0000-99-1 HSP-PM through hole stand off

8 Important Technology Information

The following technological information is designed to give the reader a better understanding of some of features of the microETXexpress™-PM. This information can be referenced when reading the System Resources and BIOS Operation sections that follow. There are also references to additionall documentation that will help to develop a better understanding of the technical information described herein.

8.1 ACPI

The microETXexpress™ supports ACPI. Non ACPI (APM support) is not intended.

8.2 I/O APIC vs 8259 PIC Interrupt mode

The I/O APIC (Advanced Programmable Interrupt Controller) handles interrupts differently then the 8259 PIC. The following information explains these differences.

8.2.1 Method of interrupts transmission

The I/O APIC transmits interrupts through the system bus and interrupts are handled without the needs for the processor to run an interrupt acknowledge cycle.

8.2.2 Interrupt priority

The priority of interrupts in the I/O APIC is independent of the interrupt number.

8.2.3 More interrupts

The I/O APIC in the chipset of the microETXexpress™-PM supports a total of 24 interrupts.

The APIC is not supported by all operating systems. Windows XP, Vista and Linux does support APIC. The APIC mode must be enabled in the BIOS setup before the OS installation. APIC only works in ACPI mode.

For more information see chapter 8 of the IA-32 Intel Architecture Software Developer's Manual, Volume 3.

Note: Enable the APIC mode if your OS supports it.

8.3 Native vs. compatible IDE mode

Windows XP SP1 and Windows Server 2003 will switch a native-mode-capable ATA controller from compatible to native mode if the BIOS indicates that the controller can be switched, the controller supports native mode and the appropriate registry entry is set. You must add a DWORD VALUE called **EnableNativeModeATA** under:

HKEY_LOCAL_MACHINE/System/CurrentControlSet/Control/PnP/Pci/

and set 1 as the value.

8.3.1 Compatible Mode

The ATA controller emulates a legacy IDE controller, which is a non-standard extension of the ISA-based IDE controller. In compatible mode, the controller requires two ISA IRQs (14 and 15) that cannot be shared with other devices.

8.3.2 Native Mode

The ATA controller acts as a true PCI device that does not require dedicated legacy resources and can be configured anywhere in the system. ATA controllers running in native mode use their PCI interrupt for both channels and can share this interrupt pin with other devices in the system, like any other PCI device.

By requiring only one shareable interrupt instead of two non-shareable ones, native-mode controllers significantly decrease the likelihood that a user will install a device that cannot work because no interrupts are available.

Enable Native IDE mode if your OS supports it. http://www.microsoft.com/whdc/device/storage/Native-modeATA.mspx

Note: For more information see: http://www.microsoft.com/whdc/device/storage/Native-modeATA.mspx

8.4 Thermal Monitor and Catastrophic Thermal Protection

The Thermal Monitor within the Pentium M processor helps to control the processor temperature by activating the TCC (Thermal Control Circuit) when the processor silicon reaches its maximum operating temperature. The temperature at which the Intel Thermal Monitor activates the TCC is not user-configurable and is not software visible.

The Thermal Monitor controls the processor temperature by modulating (starting and stopping) the CPU core clocks at a 50% duty cycle (TM1) or by initiating an Enhanced Intel Speedster technology transition (TM2) when the processor silicon reaches its maximum operating temperature (selectable in setup).

Note: TM2 is the recommended mode for the Intel Pentium M processor.
Not supported on the microETXexpress™-PM Celeron 0.8 GHz and 1.0 GHz.

Thermal Monitor supports two modes to activate the TCC: Automatic and On-Demand mode. The Intel Thermal Monitor Automatic Mode must be enabled via BIOS for the processor to be operating within specification.

Automatic mode does not require any additional hardware, software drivers, or interrupt handling routines.

Note: With a properly designed thermal solution, the TCC is only active for very short periods, hence processor performance impact is expected to be so minor that it would not be detectable.
For more details see chapter 5.1.2 of the Intel Pentium M Processor Datasheet.

The Intel Pentium M processor supports the THERMTRIP# signal for catastrophic thermal protection.

In the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached a temperature of approximately 125°C. At this point the system BUS signal THERMTRIP# will go active.

THERMTRIP# activation is independent of processor activity and does not generate any bus cycles.

8.4.1 Summary

Thermal Control Circuit reduces performance when the processor reaches its max. operating temperature (100°C). THERMTRIP# shuts down the system in case of catastrophic cooling failure.

8.5 Processor Performance Control

The Pentium M processor can run in different performance states (multiple frequency/voltage operating points). The CPU performance can be altered while the computer is functioning. This allows the processor to run at different core frequencies and voltages depending on CPU thermal state and OS policy.

Windows XP includes built-in processor performance control to operate the processor more efficiently when it is not fully utilized. Win2k, WinME and Win9x do not support processor performance control. Special software is required for Oses not capable of processor performance control.

In Windows, the processor performance control policy is linked to the Power Scheme setting in the control panel power option applet.

Note: Windows always runs at the highest performance state when the "Home/Office" or "Always On" power scheme is selected.
For a more detailed information about processor performance control, see:
Chapter 8 of the ACPI Specification Revision 2.0c available at www.acpi.info

ACPI allows the OS to play a role in the thermal management of the system. With the OS in control of the operating environment, cooling decisions can be made based on the application load on the CPU and the thermal heuristics of the system.

Note: Linux also includes processor performance control built-in for efficient use of the System and also supports ACPI working mode.

8.5.1 Cooling Policies

The ACPI thermal solution on microETXexpress™-PM supports two cooling policies:

Passive Cooling

The OS reduces the power consumption of the processor by throttling the processor clock to reduce the temperature of the thermal zone. Passive cooling devices (processor) produce no noise. The passive cooling trip point declares the temperature threshold where the OS will start or stop passive cooling.

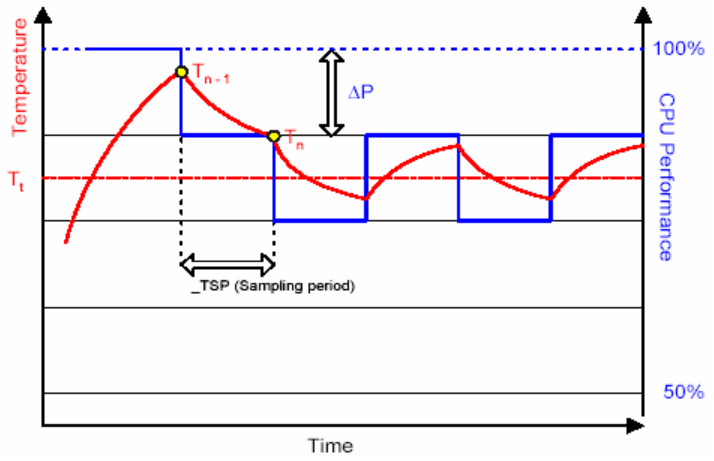
Critical Trip Point

The OS performs an orderly, but critical, shutdown of the system when the temperature reaches the critical trip point.

Note: Customers can design there own fan cooling methode (on the Backplane) which is not SW controlled.

8.6 Processor Clock Throttling

The ACPI OS assesses the optimum CPU performance change necessary to lower the temperature using the following equation:



$\Delta P[\%] = TC1(Tn-Tn-1) + TC2(Tn-Tt)$

ΔP is the performance delta, Tt is the target temperature = passive cooling trip point. The two coefficients TC1 and TC2 and the sampling period TSP are hardware dependent constants the end user must supply (setup options section ACPI Control Submenu).

It's up to the end user to set the cooling preference of the system by setting the appropriate trip points in the BIOS setup.

Note: See chapter 12 of the ACPI specification (www.acpi.info) for more details.

8.7 ACPI Suspend Modes and Resume Events

The microETXexpress™-PM supports the S1 (POS=Power On Suspend) state. S3 (=Save to Ram) is supported.

S4 (=Save to Disk) is not supported by the BIOS (S4_BIOS) but it is supported by the following operating systems:

- WinME
- Win2k
- WinXP (S4_OS=Hibernate)

The following events resume the system from S1:

- Power Button
- PS/2 Keyboard and Mouse IRQs (1 & 12)
- USB Wake Events
- PCI Bus signal PME#

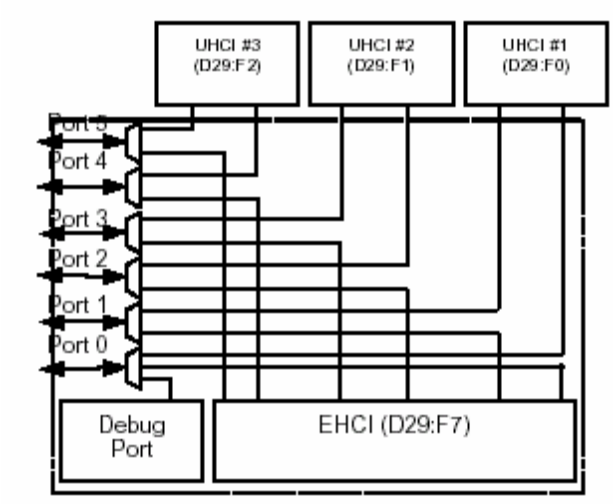
The following events resume the system from S3:

- Power Button
- LAN activities (tested wiht magic packet)

8.8 USB 2.0 (EHCI) Host Controller Support

The EHCI host controller shares the 6 USB ports with the 3 UHCI host controllers. Integrated into the EHC functionality is a port-routing logic, which performs the mixing between the UHCI and EHCI host controllers. If a device is connected that is not capable of USB2.0's high-speed signaling protocol, or if the EHCI software drivers are not present, than the UHCI controller owns the ports.

Routing Diagram:



Note: USB2.0 high speed boot is supported by the BIOS.

9 System Resources

9.1 Interrupt Request (IRQ) Lines

In 8259 PIC mode

IRQ #	Used For	Available	Comment
0	Timer0	No	
1		Yes	
2	Slave 8259	No	
3	COM2	No	Note (2)
4	COM1	No	Note (2)
5		Yes	
6		Yes	
7		Yes	
8	RTC	No	
9	SCI	No	Note (3)
10		Yes	
11		Yes	
12		Yes	
13	FPU	No	
14	IDE0	No	Note (1)
15		Yes	

Note: 1 If the "Used For" device is disabled in setup, the corresponding interrupt is available for other devices.
2 Unavailable if baseboard is equipped with an LPC-I/O controllerWinbond W83627HF, and the device is enabled in setup.
3 Unavailable in Advanced Configuration and Power Interface (ACPI) mode. Used as System Control Interrupt (SCI) in ACPI mode.

In APIC mode:

IRQ #	Used For	Available	Comment
0	Timer0	No	
1		Yes	
2	Slave 8259	No	
3	COM2	No	Note (1)
4	COM1	No	Note (1)
5		Yes	
6		Yes	
7		Yes	
8	RTC	No	
9	SCI	No	System Control Interrupt (2)
10		Yes	
11		Yes	
12		Yes	
13	FPU	No	
14	IDE0	No	Note (3)
15		Yes	
16	PIRQ[A]	For PCI	PCI IRQ line 1 + USB UCHI controller #1 + Graphics controller
17	PIRQ[B]	For PCI	PCI IRQ line 2 + AC97 Audio controller
18	PIRQ[C]	For PCI	PCI IRQ line 3 + USB UCHI controller #3 + Native IDE
19	PIRQ[D]	For PCI	PCI IRQ line 4 + USB UCHI controller #2
20	PIRQ[E]	No	Lan Controller
21	PIRQ[F]	No	
22	PIRQ[G]	No	SATA controller
23	PIRQ[H]	No	USB EHCI controller

Note: 1 Unavailable if baseboard is equipped with an LPC I/O controllerWinbond W83627HF, and the device is enabled in setup.
2 Unavailable in Advanced Configuration and Power Interface (ACPI) mode. Used as System Control Interrupt (SCI) in ACPI mode. Currently not free in Non-ACPI mode.
3 IRQs are available if IDE controller is either disabled in setup or if in Native IDE mode.

9.2 Direct Memory Access (DMA) Channels

DMA #	Used for	Available	Comment
0		Yes	
1		Yes	
2		Yes	
3		Yes	
4	Cascade	No	
5		Yes	
6		Yes	
7		Yes	

9.3 Memory Area

Upper Memory	Used for	Available	Comment
C0000h – CFFFFh	VGA BIOS	No	
D0000h – DFFFFh		Yes	Shadow RAM
E0000h – FFFFFh	System BIOS	No	

9.4 I/O Address Map

The I/O-port addresses of the microETXexpress™-PM are functionally identical with a standard PC/AT.

The following I/O ports are used:

I/O Address	Used for	Available	Comment
3F8-3FFh	COM1	No	Available if external I/O controller not used.
2F8-2FFh	COM2	No	Available if external I/O controller not used.
1000h >	PCI	No	I/O ports 1000h and above might be allocated by PCI devices or onboard hardware.

9.5 Peripheral Component Interconnect (PCI) Devices

PCI Device	Busmaster	PCI Interrupt	Comment
Audio, USB and Ethernet		See IRQ resource tables above	Integrated in the Intel chipset. No REQx/GNTx pair needed.
SATA		See IRQ resource tables above	Serial ATA Controller. REQ4/GNT4 used for it.

You can use REQ0/GNT0, REQ1/GNT1, REQ2/GNT2, and REQ3/GNT3 pairs for external PCI devices.

9.6 Inter-IC (I2C) Bus

I2C Address	Used For	Available	Comment	JIDA-Bus-Nr.
A0h	JIDA-EEPROM	No	EEPROM for CMOS data.	0
A2h	JIDA-EEPROM	No		0
B0h	WD-PIC	No	Reserved for internal use.	0

9.7 System Management (SM) Bus

Following SM bus addresses are reserved.

SM Bus Address	SM Device	Comment	JIDA-Bus-Nr.
10h	SMB Host	Do not use under any circumstances.	1
12h	SMART_CHARGER	Not to be used with any SM bus device except a charger	1
14h	SMART_SELECTOR	Not to be used with any SM bus device except a selector	1
16h	SMART_BATTERY	Not to be used with any SM bus device except a battery	1
A0h	SPD	SDRAM EEPROM	1
D2h	Clock generator	Do not use under any circumstances.	1

The standard microETXexpress™-PM Power management BIOS does support MARS (**M**obile **A**pplication platform for **R**echargeable **S**ystems). Further details about MARS are available at Embedded Modules Division - Kontron.

9.8 JILI-I2C Bus

I2C Address	Used For	Available	Comment	JIDA-Bus-Nr.
A0h	JILI-EEPROM	No	EEPROM for JILI-Data	2

10 BIOS Operation

The module is equiped with a Phoenix legacy **Reduced** Bios. This implicates that the Module works only in ACPI-Mode. The Bios is located in an onboard Flash EEPROM. The device has 8-bit access. Faster access (16 bit) is provided by the shadow RAM feature. You can update the BIOS using a Flash utility.

The Legacy **Reduced** Bios has been developed on demand of many OEM in order to lower system and support cost. Removal of obsolete, slow, complicated, and often poorly understood interfaces provides obvious benefits toward this goal: simpler, more robust machines, and a lower cost of goods.

As a result of these initiatives, the operating system (OS), devices, and end users cannot detect the presence of the following:

- ISA bus, slots or devices;
- legacy floppy disk;
- controller (FDC);
- PS/2 and game ports.

10.1 Determining the BIOS Version

To determine the PhoenixBIOS version, immediately press the Pause key on your keyboard as soon as you see the following text display in the upper left corner of your screen:

PhoenixBIOS 4.0 Release 6.1.X.XX

Copyright 1985-2006 Phoenix Technology Ltd

All Rights Reserved

Kontron® BIOS Version <EEB1R110>

© Copyright 2002-2007 Kontron Embedded Modules GmbH

10.2 Setup Guide

The PhoenixBIOS Setup Utility changes system behavior by modifying the BIOS configuration. The setup program uses a number of menus to make changes and turn features on or off.

The BIOS setup menus documented in this section represent those found in most models of the microETXexpress™-PM. The BIOS Setup for specific models can differ slightly.

Note: Selecting incorrect values may cause system boot failure. Load setup default values to recover by pressing <F9>. It might also be necessary to use the "reset configuration data" option in the BIOS setup and set it to "yes". In certain circumstances this may also help to recover from system boot failure or a resource conflict.

10.2.1 Start Phoenix BIOS Setup Utility

To start the PhoenixBIOS setup utility, press <F2> when the following string appears during bootup.

Press <F2> to enter Setup

The Info Menu then appears.

The Setup Screen is composed of several sections:

Setup Screen	Location	Function
Menu Bar	Top	Lists and selects all top level menus.
Legend Bar	Bottom	Lists setup navigation keys.
Item Specific Help Window	Right	Help for selected item.
Menu Window	Left Center	Selection fields for current menu.
General Help Window	Overlay (center)	Help for selected menu.

Menu Bar

The menu bar at the top of the window lists different menus. Use the left/right arrow keys to make a selection.

Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. The table below describes the legend keys and their alternates.

Key	Function
<F1> or <Alt-H>	General Help window.
<Esc>	Exit menu.
← or → Arrow key	Select a menu.
↑ or ↓ Arrow key	Select fields in current menu.
<Tab> or <Shift-Tab>	Cycle cursor up and down.
<Home> or <End>	Move cursor to top or bottom of current window.
<PgUp> or <PgDn>	Move cursor to next or previous page.
<F5> or <->	Select previous value for the current field.
<F6> or <+> or <Space>	Select next value for the current field.
<F9>	Load the default configuration values for this menu.
<F10>	Save and exit.
<Enter>	Execute command or select submenu.
<Alt-R>	Refresh screen.

Selecting an Item

Use the ↑ or ↓ key to move the cursor to the field you want. Then use the + and – keys to select a value for that field. The Save Value commands in the Exit menu save the values displayed in all the menus.

Displaying Submenus

Use the ← or → key to move the cursor to the submenu you want. Then press <Enter>. A pointer (▸) marks all submenus.

Item Specific Help Window

The Help window on the right side of each menu displays the Help text for the selected item. It updates as you move the cursor to each field.

General Help Window

Pressing <F1> or <Alt-F1> on a menu brings up the General Help window that describes the legend keys and their alternates. Press <Esc> to exit the General Help window.

10.3 Main Menu

Feature	Option	Description
System Time	HH:MM:SS	Set system time. Use <Enter to move to MM or SS.
System Date	MM/DD/YYYY	Set system date. Use <Enter to move to DD or YYYY.
‣ Primary Master	Autodetected drive	Displays result of PM autotyping.
‣ Primary Slave	Autodetected drive	Displays result of PS autotyping.
Smart Device Monitoring	Disabled **Enabled**	IDE Failure Prediction.Turns on Self-Monitoring Analysis-Reporting Technology, which monitors the condition of the hard drive and reports when a catastrophic IDE failure is about to happen.
System Memory	N/A	Displays amount of conventional memory detected during bootup.
Extended Memory	N/A	Displays amount of extended memory detected during bootup.
BIOS Date	MM/DD/YY	Build Date of the BIOS
LAN1 MAC address	XX:XX:XX:XX:XX	Physical address of the onboard LAN controller

Note: In the Option column, bold shows default settings.

10.3.1 Master or Slave Submenus

Feature	Option	Description
Type	None IDE Removable ATAPI Removable CD-ROM Other ATAPI User **Auto**	None = Autotyping is not able to supply the drive type or end user has selected None, disabling any drive that may be installed. User = You enter parameters of hard-disk drive installed at this connection. Auto = Autotypes hard-disk drive installed here. CD-ROM = A CD-ROM drive is installed here. ATAPI Removable = Removable disk drive is installed here.
Cylinders	1 to 65,536	Number of cylinders.
Heads	1 to 256	Number of read/write heads.
Sectors	1 to 63	Number of sectors per track.
Maximum Capacity	N/A	Displays the calculated size of the drive in CHS
Total Sectors	N/A	Number of total sectors in LBA mode
Maximum Capacity	N/A	Displays the calculated size of the drive in LBA
Multi-Sector Transfer	Disabled 2 sectors 4 sectors 8 sectors **16 sectors**	Any selection except Disabled determines the number of sectors transferred per block. Standard is 1 sector per block.
LBA Mode Control	Disabled **Enabled**	Enabling LBA causes Logical Block Addressing to be used in place of CHS.
32-Bit I/O	**Disabled**	Enables 32-bit communication between CPU and IDE card. Requires PCI or

Feature	Option	Description
	Enabled	Local Bus.
Transfer Mode	Standard Fast PIO 1 Fast PIO 2 Fast PIO 3 Fast PIO 4 FPIO 3/ DMA 1 FPIO 4/ DMA 2	Selects the method for transferring the data between the hard disk and system memory.
Ultra DMA Mode	Disabled Mode 0 Mode 1 Mode 2 Mode 3 Mode 4 Mode 5	Selects the UDMA mode used for moving data to/from the drive. Autotype the drive to select the optimum transfer mode.
SMART Device Monitoring	Disabled Enabled	Shows if SMART Device monitoring is supported by the drive.

10.4 Advanced Menu

Feature	Option	Description
▸ Advanced Chipset Control	sub menu	Opens Advanced Chipset Control sub menu.
▸ PCI/PNP Configuration	sub menu	Opens PCI/PNP Config sub menu.
▸ Memory Cache	sub menu	Opens Cache Control sub menu.
▸ I/O Device Configuration	sub menu	Opens Peripheral Config sub menu.
▸ Keyboard Features	sub menu	Opens Keyboard Features sub menu.
▸ Hardware Monitor	sub menu	Shows hardware monitor current state.
▸ Watchdog Settings	sub menu	Opens Watchdog Config sub menu.
▸ Display Control	sub menu	Opens Display Control sub menu
▸ Miscellaneous	sub menu	Opens sub menu with miscellaneous options.

Note: Setting items on this menu to incorrect values may cause your system to malfunction.

10.4.1 Advanced Chipset Control Submenu

Feature	Option	Description
Graphics Engine 1	Disabled **Enabled**	Enable/Disable Internal Graphics Device.
Graphics Engine 2	Disabled **Enabled**	Enabled/Disabled Function 1 of the Internal Graphics Device
Graphics Memory	1MB, **8MB**, 16MB, 32MB UMA	Select the amount of main memory that the Internal Graphics Device will use.
Assign IRQ to VGA	Disabled **Enabled**	Determines whether the VGA Device gets an IRQ assigned.

Note: In the Option column, bold shows default settings.

10.4.2 PCI/PNP Configuration Submenu

Feature	Option	Description
Plug & Play OS	No **Yes**	Select the operating system installed on your system which you will use most commonly. If your system has a PnP OS (e.g. Win9x) select Yes to let the OS configure PnP devices not required for booting. No allows the BIOS to configure them. Note: An incorrect setting can cause some operating systems to display unexpected behaviour.
Reset Configuration Data*	**No** Yes	Yes erases all configuration data in ESCD, which stores the configuration settings for plug-in devices. Select Yes when required to restore the manufacturer's defaults.
Secured Setup Configuration	**Yes** No	Yes prevents a Plug and Play OS from changing system settings.
‣ PCI Device, Slot #x	sub menu	Opens sub menu to configure slot x PCI device
PCI IRQ line 1 PCI IRQ line 2 PCI IRQ line 3 PCI IRQ line 4 Onboard LAN IRQ line Onboard EHCI IRQ line	Disabled **Auto** IRQ3, 4, 5, 7, 9, 10, 11, 12, 14,15	PCI devices can use hardware interrupts called IRQ´s. A PCI device cannot use IRQ´s already in use by ISA or EISA devices. Use "Auto" only if no ISA or EISA legacy cards are installed.
Default Primary Video Adapter	**AGP** PCI	Select "PCI" to have a PCI video card, if installed, used for the boot display device. Select "AGP" to have a AGP video card, if installed, used for the boot display device.
Assign IRQ to SMB	Disabled **Enabled**	Determines whether the onchip SMBus host controller gets an IRQ assigned.

Note: In the Option column, bold shows default settings.
**Setting this option to "yes", under certain circumstances, may help to recover from system boot failure or a resource conflict.*

PCI Device, Slot # x Submenu

Feature	Option	Description
Option ROM Scan	Disabled **Enabled**	Initialize device expansion ROM.
Enable Master	**Disabled** Enabled	Enables device in slot as a PCI bus master, not every device can function as a master. Check device documentation.
Latency Timer	**Default,** 20h, 40h, 60h, 80h, A0h, C0h, E0h	Minimum guaranteed time slice allocated for bus master in units of PCI bus clocks. A high-priority, high-throughput device may benefit from a greater value.

Note: In the Option column, bold shows default settings.

10.4.3 Memory Cache Submenu

Feature	Option	Description
Memory Cache	Disabled **Enabled**	Enables or Disables the L2 cache.
Cache System BIOS area	uncached **Write Protect**	Controls caching of System BIOS area.
Cache Video BIOS area	uncached **Write Protect**	Controls caching of Video BIOS area.
Cache Base 0 – 512k	Uncached Write Through Write Protect **Write Back**	Controls caching of 512k base memory.
Cache Base 512 – 640k	Uncached Write Through Write Protect **Write Back**	Controls caching of 512k – 640k base memory.
Cache Extended Base / Extended Memory area:	uncached Write Through Write Protected **Write Back**	Controls caching of system memory below 640k / above 1MB.
D000 – D3FF D400 – D7FF D800 – DBFF DC00 – DFFF	**Disabled** Write Through Write Protected Write Back	Disabled: block is not cached. Write Through: Writes are cached and sent to main memory at once. Write Protect: Writes are ignored. Write Back: Writes are cached, but not sent to main memory until necessary.

Note: In the Option column, bold shows default settings.

10.4.4 I/O Device Configuration Submenu

Feature	Option	Description
Primary IDE UDMA66/100	**Enabled** Disabled	Disabled limits max. transfer mode to UDMA33. Enabled allows UDMA66 and above.
SATA controller	**Enabled** Disabled	Enable/Disable the onboard SATA controller
▸ USB Options	sub menu	Opens USB sub menu.
AC97 Audio Controller	Disabled **Enabled**	Enable the AC97 Audio device. This Setup Item will have no effect if an AC97 Audio MDC is not present.
Onboard LAN controller	**Enabled** Disabled	Enable/Disable the ICH4 internal LAN controller. Setting item to "Disable" will remove the LAN from PCI Config Space.
Onboard LAN PXE ROM	**Disabled** Enabled	Enables the remote boot BIOS extension for the onboard LAN controller.
*Serial port A: *Serial port B:	**Disabled** Enabled Auto	Configure serial port: Disabled: No configuration Enabled: User Configuration Auto: BIOS or OS chooses configuration
Base I/O address	3F8h, 2F8h, 3E8h, 2E8h	Select I/O base of port.
IRQ (port A and B)	IRQ 3, IRQ 4	Select IRQ of port A and B

Parallel port:	**Disabled** Enabled Auto	Configure parallel port using options: Disabled: No configuration Enabled: User Configuration Auto: BIOS or OS chooses configuration
Mode:	Output only Bi-directional EPP **ECP**	Set the mode for the parallel port
Base I/O address	**378** 278 3BC	Set the base I/O address for the parallel port.
Interrupt	IRQ 5 **IRQ 7**	Set the interrupt for the parallel port.
DMA channel	DMA 1 **DMA 3**	Set the DMA channel for the parallel port.

Notes: In the Option column, bold shows default settings.
**Available if an external Super I/O (Winbond W83627HF) is on the base board.!*

USB Sub menu

Feature	Option	Description
USB UHCI Host Controller 1	**Enabled** Disabled	Enable/ Disable UHCI 1 HC = USB ports 0 and 1.
USB UHCI Host Controller 2	**Enabled** Disabled	Enable/ Disable UHCI 2 HC = USB ports 2 and 3.
USB UHCI Host Controller 3	**Enabled** Disabled	Enable/ Disable UHCI 3 HC = USB ports 4 and 5.
USB EHCI Host Controller *	**Enabled** Disabled	Control USB 2.0 functionality through this Setup Item. If enabled, Ports 0 - 5 are multiplexed between UHCI and EHCI. Ports are routed to EHCI if an USB2.0 high speed device is connected and an EHCI driver is loaded.

Notes: In the Option column, bold shows default settings.
**The USB ports are multiplexed between UHCI and EHCI. Ports are routed to EHCI if an USB 2.0 high-speed device is connected and an EHCI driver is loaded.*

10.4.5 Keyboard Features Submenu

Feature	Option	Description
Numlock	**Auto** On Off	On or Off turns NumLock on or off at bootup. Auto turns NumLock on if it finds a numeric key pad.
Key Click	**Disabled** Enabled	Turns audible key click on.
Keyboard auto-repeat rate	**30/sec**,26.7/sec, 21.8/sec, 13.3/sec, 10/sec, 6/sec, 2/sec	Sets number of times to repeat a keystroke per second if you hold the key down.
Keyboard auto-repeat delay	¼ sec, **½ sec**, ¾ sec, 1 sec	Sets delay time after the key is held down before it begins to repeat the keystroke.

Note: In the Option column, bold shows default settings.

10.4.6 Hardware Monitor Submenu

This submenu shows the current voltages and temperatures of the system.

Vcc (3.3)	3.3V power plane
CPU core Voltage	Core voltage (depends on CPU)
5Vsb Voltage	5 V stand by
Battery Voltage	Backup Battery Voltage
CPU Temperature	Temperature of CPU die

10.4.7 Watchdog Settings Submenu

Feature	Option	Description
Mode	**Disabled** Reset NMI	Select watchdog operation mode.
Delay	1s, 5s, 10s, **30s**, 1min, 5.5min,10.5min, 30.5min	The time until the watchdog counter starts counting. Useful to handle longer boot times.
Timeout	1s, 5s, 10s, **30s**, 1min, 5.5min, 10.5min, 30.5min	Maximum trigger period.

Note: In the Option column, bold shows default settings.

10.4.8 Display Control Submenu

Feature	Option	Description
Display Mode	CRT only LFP only **CRT+LFP**	Select the display mode.
JDA Revision	1.5	Displays the revision of the JILI data area image.
Flat Panel Type	VGA 1x18 SVGA 1x18 XGA 1x18 XGA 1x24 XGA 2x18 SXGA 2x24 UXGA 2x18 Enter PAID Enter FPID **Auto**	Select Auto to let the BIOS automatically detect the panel type or use one of the predefined fixed panel types. Choose Enter PAID or Enter FPID to manually set JILI3 ID values.
*PAID/FPID1	0 – FFFF, **default 0**	Enter the JILI3 ID.
Flat Panel Scaling	Centered **Stretched**	Stretched expands a low resolution video mode to full screen on a higher flat panel resolution.
**Flat Panel Backlight	0 – 255, default 128	Enter a value to adjust backlight of the LCD.
***Flat Panel Contrast	0 – 63, default 32	Enter a value to adjust contrast of the LCD.

Notes: **Only available if Flat Panel Type (Enter PAID) or (Enter FPID) are selected.*
***Only available if the DAC (MAX5362) is on the OEM backplane or the panel adapter.*
****Only available if the digitally controlled potentiometer (Xicor X9429) is on the OEM backplane or the panel adapter.*

10.4.9 Miscellaneous Submenu

Feature	Option	Description
Floppy Check	**Disabled** Enabled	Enabled verifies floppy type on boot; disabled speeds boot.
Summary Screen	**Disabled** Enabled	If enabled, a summary screen is displayed just before booting the OS to let the end user see the system configuration.
QuickBoot Mode	Disabled **Enabled**	Allows the system to skip certain tests while booting. This will decrease the time needed to boot the system.
Extended Memory Testing	Normal **Just zero it** None	Determines which type of tests will be performed on memory above 1MB. The option Normal is not visible if QuickBoot is enabled.
Dark Boot	**Disabled** Enabled	If enabled, system comes up with a blank screen instead of the diagnostic screen during bootup.
Halt On Errors	**Yes** No	Determines if post errors cause the system to halt.
Large Disk Access Mode	**DOS** Other	Select DOS if you have DOS. Select Other if you have another OS such as UNIX. A large disk is one that has more than 1024 cylinders, more than 16 heads or more than 63 sectors per track.
Additional Boot Delay	**Not allow** Other	Add 3sec Delay to Start of POST. This is useful for some Devices to be Autotyped by System Bios, especially some USB HDDs.

10.5 Security Menu

Feature	Option	Description
Supervisor Password Is:	**Clear** Set	If a password is choosen "Set" will appear in this field.
User Password Is:	**Clear** Set	If a password is choosen "Set" will appear in this field.
Set Supervisor Password	Up to seven alphanumeric characters	Pressing <Enter> displays the dialog box for entering the user password. In related systems, this password gives full access to setup.
Set User Password	Up to seven alphanumeric characters	Pressing <Enter> displays the dialog box for entering the user password. In related systems, this password gives restricted access to setup.
*Diskette access	User Supervisor	Enabled requires supervisor password to access floppy disk.
Fixed disk boot sector	**Normal** Write protected	Write protect the boot sector on the hard disk for virus protection. Requires a password to format or Fdisk the hard disk.
Virus check reminder System backup reminder	**Disabled** Daily	Displays a message during bootup asking (Y/N) if you backed up the system or scanned for viruses.

	Weekly Monthly	Message returns on each boot until you respond with „Y“. Daily displays the message on the first boot of the day, Weekly on the first boot after Sunday, and Monthly on the first boot of the month.
**Password on boot	**Disabled** Enabled	Enabled requires a password on boot. Requires prior setting of the supervisor password. If supervisor password is set and this option is disabled, BIOS assumes user is booting.
**Password on bootmenu	**Disabled** Enabled	Enables password entry on bootmenu.

Notes: In the Option column, bold shows default settings.
Enabling Supervisor Password requires a password for entering Setup.
Passwords are not case sensitive.
User and Supervisor passwords are related.
**Appears when User/Supervisor password is choosen and Password on boot is enabled.*
***Available only when a User/Supervisor password is choosen.*

10.6 Power Menu

A power management system reduces the amount of energy used after specified periods of inactivity. The setup menu supports:

- ➤ Full On state
- ➤ Standby state with partial power reduction
- ➤ Suspend state with full power reduction

Use the Advanced Options menu to specify whether an activity can terminate a Standby or Suspend state and restore Full On.

Feature	Option	Description
*ACPI Control	sub menu	These items will control selective functionality when an ACPI OS is loaded.
*Automatic Thermal Control Circuit	Disabled TM1 **TM2**	Enables the thermal control circuit (TCC) of the thermal monitor feature of the Pentium-M CPU. TM1 = 50% duty cycle TM2 = Geyserville III Automatic TTC must be enabled to ensure that the processor operates within specification.
**Max CPU frequency	**1400 MHz** 1300 MHz 1200 MHz 1100 MHz 1000 MHz 900 MHz 800 MHz 600 MHz	Warning! Selecting frequencies higher then the default may cause the system to reach “critical trip point” and shutdown if a proper cooling solution is not used. Always ensure that you use proper cooling when selecting higher frequency settings.
Resume on Modem Ring	**Off** On	Enabled wakes the system on incoming calls detected by modem (RI).
Resume on Time	**Off** On	Enabled wakes the system at a specific time.

Resume Time	00:00:00	Specify the time when the system is to wake up. <Tab>, <Shift-Tab> or <Enter> selects field.
Power Supply	**ATX** AT	Choose the connected power supply, ATX or AT.
Power Button Function	**Power Off** Sleep	Determines if the system enters suspend or soft off when the power button is pressed.
Power Loss Control	Stay Off Power On **Last State**	Determines how the system behaves after a power failure. This only works in conjunction with a CMOS backup battery.
Enable PME for WOL	**OS control** Enabled Disabled	This item controls the activation of the PME line which can be used to wake the system via LAN. OS control: BIOS won´t interfere with the settings made in an ACPI OS.

Notes: In the Option column, bold indicates default setting.
** See Important Technology Information of this user's guide for more details about ACPI.*
***The CPU frequency values shown in this example are taken from the microETXexpress™-PM 1.4GHz. Please note that other microETXexpress™-PM variants capable of CPU frequency switching may have different possible values listed as well as different defaults*

10.6.1 ACPI Control sub menu

Feature	Option	Description
*Deepest sleep state for standby	None **S1** S3	*S3 saves more power than S1 and choosing "None" will disable standby in the OS. Please be sure your board support the appropriate Sleep state when making this choice.
Passive Cooling Trip Point	**Disabled** 40 C – 100 C	Determines the temperature of the ACPI Passive Trip Point, the point at which the OS will turn on/off CPU clock throttling.
Passive TC1 Value	**1**, 2, 3, ...15, 16	Determines the TC1 (temperature coefficient 1) value for the ACPI passive cooling formula. See section 8.6 Processor Clock Throttling.
Passive TC2 Value	1, 2, 3, 4, **5**, ...15, 16	Determines the TC2 (temperature coefficient 2) value for the ACPI passive cooling formula. See section 8.6 Processor Clock Throttling.
Passive TSP Value	2, 4, 6, 8, **10**, ... 28, 30	Determines the Tsp (sampling period) value for the ACPI passive cooling formula. See chapter 8.6 Processor Clock Throttling.
Critical Trip Point	40 C – 110 C	This value controls the temperature of the ACPI Critical Trip Point- the point at which the OS will shut the system off.
APIC – IO APIC Mode	**Disabled** Enabled	This item is valid only for Windows XP. Also, a fresh install of the OS must occur when APIC Mode is desired Test the IO APIC by setting an item to Enabled. The APIC Table will then be pointed to by the RSDT, the Local APIC will be initialized, and the proper enable bits will be set in IHC4M. See section 8.1ACPI The microETXexpress™ supports ACPI. Non ACPI (APM support) is not intended. I/O APIC vs 8259 PIC Interrupt mode
Native IDE Support	**Disabled** Enabled	Enable Native IDE support for WINXP by setting this item. The NATA Package will be created if this item is set to Enabled. Changing this item will have no effect in WIN98, WINME, or

		WIN2K. See section 8.3 Native vs. compatible IDE mode for more details.
IGD - S3 Popup	**Disabled** Enabled	If the IGD is the primary display device and this option is set to enabled, a Popup Icon will be displayed for 5 seconds during ACPI S3 resume.

ACPI Resume Events

microETXexpress™-PM supports S1 state , S3 (S2R) and S4 (S2D). The following events resume the system from S1:

- Power button
- PME#
- USB keyboard and mouse activity
- USB resume event

The following event resume the system from S3:

- Power button
- LAN activities (tested wiht magic packet)

Notes	*In the Option column, bold indicates default setting.* **Available when ACPI is switched off.* *Automatic TTC must be enabled to ensure that the processor operates within specificaion.* *** The microETXexpress™-PM Celeron M default setting for this value is TM1 because the microETXexpress™-PM Celeron M does not support TM2.*

10.7 Boot Menu

10.7.1 MultiBoot

Multiboot allows you to select the following boot devices:

- Hard disk
- Floppy disk
- CD-ROM
- Network card

You can make the selections from Setup, or by selecting the boot device in the BootFirst Menu.

Note: The microETXexpress™-PM also supports booting from USB floppy and Mass Storage Device (MSD).

MultiBoot consists of the 2 menus:

- Setup Boot Menu
- Boot First Menu

10.7.2 The Setup Boot Menu

This menu allows selecting the order of the devices from which the BIOS attempts to boot the OS. During POST, if BIOS is unsuccessful at booting from one device, it will try the next one on the list.

The Boot Menu shows two lists, the boot priority list and the exclude from boot order list. The sample below shows the default configuration.

	Item Specific Help
Boot Priority order: 1. IDE0: <primary master device> 2. IDE1: <primary slave device> 3. IDE CD: <IDE CD-ROM> 4. PCI SCSI: <PCI SCSI device>* 5. USB Key: <USB stick> 6. USB CDROM: <USB CD-ROM device> 7. 8. Exclude from boot order: USB FDC: <USB Floppy drive> USB HDD: <USB Hard Drive device> USB ZIP: <USB ZIP drive> USB LS-120: <USB CDROM device> PCI BEV: <PCI LAN device> Bootable Add-in Cards	Keys used to view or configure devices: Up and Down arrows select a device. <+> and <-> moves the device up or down. <f> and <r> specifies the device fixed or removable. <x> exclude or include the device to boot. <Shift + 1> enables or disables a device. <1 – 4> Loads default boot sequence.

Notes: The BIOS only tries to boot from the devices (max 8) in the Boot Priority Order list.
**SATA devices.*

10.7.3 Boot First Menu

Display the Boot First Menu by pressing <Esc> during POST. In response, the BIOS displays the message Entering Boot Menu and then displays the Boot Menu at the end of POST.

Use the menu to select one of the following options:

- Override the existing boot sequence (for this boot only) by selecting another boot device. If the specified device does not load the OS, the BIOS reverts to the previous boot sequence.
- Enter Setup.
- Press <Esc> to continue with the existing boot sequence.

10.8 Exit Menu

The following sections describe the five options in Exit Menu. Pressing <Esc> does not exit this menu. You must select an item from the menu to exit.

Exit Saving Changes

Saves all selections and exits setup. Upon reboot, the BIOS configures the system according to the Setup selection stored in CMOS.

Exit Discarding Changes

Use this option to exit Setup without storing new selections in CMOS. Previous selections remain in effect.

Load Setup Defaults

Select to display the default values for all Setup menus.

Discard Changes

Discards changes made during a Setup session and revert to values previously saved in CMOS.

Save Changes

Saves all selections without exiting Setup.

10.9 Updating or Restoring BIOS

Phoenix Phlash16 allows you to update or restore the BIOS with a newer version or restore a corrupt BIOS by using a floppy disk without having to install a new ROM chip.

➤ Get the Phoenix Phlash16 compressed file, CRDxMODB.ZIP, from the Kontron Embedded Modules GmbH. It contains the following files:

File	Purpose
MAKEBOOT.EXE	Creates the custom boot sector on the Crisis Recovery Diskette.
CRISBOOT.BIN	Serves as the Crisis Recovery boot sector code.
MINIDOS.SYS	Allows the system to boot in Crisis Recovery Mode.
PHLASH16.EXE	Programs the Flash ROM.
WINCRISIS.EXE	Creates the Crisis Recovery Diskette from Windows.
WINCRISIS.HLP	Serves as the help file of WINCRISES.EXE.
BIOS.WHP	Serves as the actual BIOS image to be programmed into Flash ROM.

➤ BIOS.WPH is a file that contains the 1MB BIOS binary and flash interface code required by Phlash16.EXE.

➤ To install Phoenix Phlash16 on a hard disk, unzip the content of CRDxMODB.ZIP into a local directory such as C:\PHLASH.

Note: Crisis Recovery requires an USB floppy drive.

➤ To create a Crisis Recovery Diskette, insert a blank diskette into Drive A: or B: and execute WINCRISIS.EXE. This copies three files onto the Crisis Recovery Diskette.

File	Purpose
MINIDOS.SYS	Allows the system to boot in Crisis Recovery Mode.
PHLASH16.EXE	Programs the Flash ROM.
BIOS.WPH	Serves as the BIOS image to be programmed into Flash ROM.

➤ If the BIOS image (BIOS.WPH) changes because of an update or bug fix, copy the new BIOS.WPH image onto the diskette.

➤ Phoenix Phlash16 runs in one of two modes: Command Line or Crisis Recovery. Use the Command Line mode to update or replace a BIOS. To execute Phlash16 in this mode, move to the Crisis Recovery Disk and type PHLASH16. Phoenix Phlash16 will update the BIOS. Phlash16 can fail if the system uses memory managers. If this occurs, the utility displays the following message:

Cannot flash when memory managers are present.

➤ If you see this message after you execute Phlash16, disable the memory manager or use parameter /x for Phlash16.exe.

10.10 Preventing Problems When Updating or Restoring BIOS

Updating the BIOS represents a potential hazard. Power failures or fluctuations that may occur during updating the Flash ROM can damage the BIOS code, making the system unbootable.

To prevent this potential hazard, many systems come with a boot-block Flash ROM. The boot-block region contains a fail-safe recovery routine. If the boot-block code finds a corrupted BIOS (checksum fails), it boots into the crisis recovery mode and loads a BIOS image from a crisis diskette (see above).

11 Appendix A: JIDA Standard

Every board with an on-board BIOS extension supports the following function calls, which supply information about the board. Jumptec Intelligent Device Architecture (JIDA) functions are called via Interrupt 15h. Functions include:

- AH=Eah
- AL=function number
- DX=4648h (security word)
- CL=board number (starting with 1)

The interrupt returns a CL≠0 if a board with the number specified in CL does not exist. CL will equal 0 if the board number exists. In this case, the content of DX determines if the operation was successful. DX=6B6Fh indicates success; other values indicate an error.

11.1 JIDA Information

To obtain information about boards that follow the JIDA standard, use the following procedure.

- Call Get BIOS ID with CL=1.
  The name of the first device installed will be returned.
  If you see the result Board exists (CL=0), increment CL, and call Get BIOS ID again.
- Repeat until you see Board not present (CL≠0).
  You now know the names of all boards within your system that follow the JIDA standard.
- You can find out more information about a specific board by calling the appropriate inquiry function with the board's number in CL.

Note: Association between board and board number may change because of configuration changes. Do not rely on any association between board and board number. Always use the procedure described above to determine the association between board and board number.

Refer to the JIDA manual in the jidai1xx.zip folder, which is available from the Kontron Embedded Modules GmbH Web site, for further information on implementing and using JIDA calls with C sample code.

12 Appendix B: Supported operating systems

The microETXexpress™-PM only works in ACPI Mode and therefore should support all Oparation Systems with ACPI capabilities.

13 Appendix C: PC Architecture Information

The following sources of information can help you better understand PC architecture.

13.1 Buses

13.1.1 ISA, Standard PS/2 – Connectors

- AT Bus Design: Eight and Sixteen-Bit ISA, E-ISA and EISA Design, Edward Solari, Annabooks, 1990, ISBN 0-929392-08-6
- AT IBM Technical Reference Vol 1&2, 1985
- ISA & EISA Theory and Operation, Edward Solari, Annabooks, 1992, ISBN 0929392159
- ISA Bus Specifications and Application Notes, Jan. 30, 1990, Intel
- ISA System Architecture, Third Edition, Tom Shanley and Don Anderson, Addison-Wesley Publishing Company, 1995, ISBN 0-201-40996-8
- Personal Computer Bus Standard P996, Draft D2.00, Jan. 18, 1990, IEEE Inc
- Technical Reference Guide, Extended Industry Standard Architecture Expansion Bus, Compaq 1989

13.1.2 PCI/104

- Embedded PC 104 Consortium
- The consortium provides information about PC/104 and PC/104-Plus technology. You can search for information about the consortium on the Web.
- PCI SIG
- The PCI-SIG provides a forum for its ~900 member companies, who develop PCI products based on the specifications that are created by the PCI-SIG. You can search for information about the SIG on the Web.
- PCI & PCI-X Hardware and Software Architecture & Design, Fifth Edition, Edward Solari and George Willse, Annabooks, 2001, ISBN 0-929392-63-9.
- PCI System Architecture, Tom Shanley and Don Anderson, Addison-Wesley, 2000, ISBN 0-201-30974-2.

13.2 General PC Architecture

- Embedded PCs, Markt&Technik GmbH, ISBN 3-8272-5314-4 (German)
- Hardware Bible, Winn L. Rosch, SAMS, 1997, 0-672-30954-8
- Interfacing to the IBM Personal Computer, Second Edition, Lewis C. Eggebrecht, SAMS, 1990, ISBN 0-672-22722-3
- The Indispensable PC Hardware Book, Hans-Peter Messmer, Addison-Wesley, 1994, ISBN 0-201-62424-9

- The PC Handbook: For Engineers, Programmers, and Other Serious PC Users, Sixth Edition, John P. Choisser and John O. Foster, Annabooks, 1997, ISBN 0-929392-36-1

13.3 Ports

13.3.1 RS-232 Serial

- EIA-232-E standard
- The EIA-232-E standard specifies the interface between (for example) a modem and a computer so that they can exchange data. The computer can then send data to the modem, which then sends the data over a telephone line. The data that the modem receives from the telephone line can then be sent to the computer. You can search for information about the standard on the Web.
- RS-232 Made Easy: Connecting Computers, Printers, Terminals, and Modems, Martin D. Seyer, Prentice Hall, 1991, ISBN 0-13-749854-3
- National Semiconductor
  The Interface Data Book includes application notes. Type “232” as search criteria to obtain a list of application notes. You can search for information about the data book on National Semiconductor’s Web site.

13.3.2 Serial ATA

- Serial AT Attachment (ATA) Working Group. This X3T10 standard defines an integrated bus interface between disk drives and host processors. It provides a common point of attachment for systems manufacturers and the system. You can search for information about the working group on the Web. We recommend you also search the Web for information on 4.2 I/O cable, if you use hard disks in a DMA3 or PIO4 mode.

13.3.3 USB

- USB Specification.
- USB Implementers Forum, Inc. is a non-profit corporation founded by the group of companies that developed the Universal Serial Bus specification. The USB-IF was formed to provide a support organization and forum for the advancement and adoption of Universal Serial Bus technology. You can search for information about the standard on the Web.

13.4 Programming

- C Programmer’s Guide to Serial Communications, Second Edition, Joe Campbell, SAMS, 1987, ISBN 0-672-22584-0
- Programmer’s Guide to the EGA, VGA, and Super VGA Cards, Third Edition, Richard Ferraro, Addison-Wesley, 1990, ISBN 0-201-57025-4

- The Programmer's PC Sourcebook, Second Edition, Thom Hogan, Microsoft Press, 1991, ISBN 1-55615-321-X
- Undocumented PC, A Programmer's Guide to I/O, CPUs, and Fixed Memory Areas, Frank van Gilluwe, Second Edition, Addison-Wesley, 1997, ISBN 0-201-47950-8

14 Appendix D: Limitations and Restrictions

- Working with a VGA PCI Card require Graphic engine 1 to be disabled
- Maximum operating temperature 0 to + 50 °C due to SATA controller

15 Appendix C: Document-Revision History

Rev.	Date	Author	Changes
1.0	16.05.07	GUL	Initial Release
		PRO	Updated HS Picture
	10.08.07	GUL	Changed Pin A35 from IO to O, B13 from O to IO, B35 from O to I, B66 from IO to I
1.1			Changed BIOS section
	17.01.08	GUL	Changed WDT B27 signal from Input to Output
			Added chipset 852 GM; Added MTBF; Updated Block Diagram